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MS-7736

ATX(Full Size)

Ver: 10

CPU:

INTEL - Sandy Bridge-E LGA2011

System Chipset:

INTEL - Patsburg PCH

OnBoard Chipset:

Clock Gen:932SQ420D + 9FGL1216AGLF
LAN:RTL 8111E 10/100/1000 NIC X 1
USB3.0: UPD720200F1 X2
Flash ROM: 8 MB SPI / 8 MB SPI (PCH)
SATA6G Controller: ASM1061

SIO:FIN71889AD(LAA)
1394 Controller: VIA6315N

Expansion Slots:

PCI Express (X16) Slot * 2
PCI Express (X8) Slot * 1
PCI Express (X1) Slot * 3

Main Memory:

DDRIII (1066/1333MHz) * 4

Other:

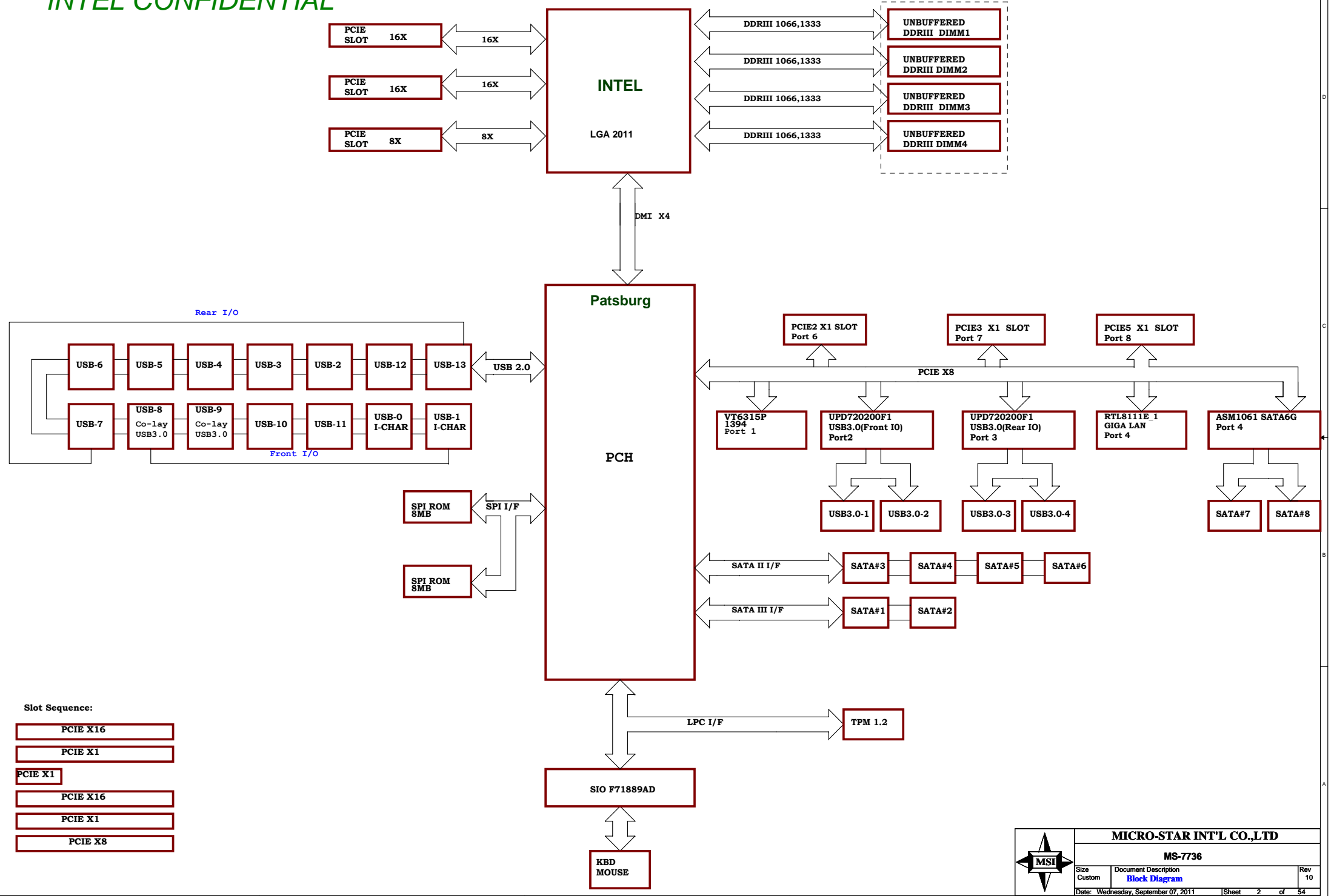
SATA3.0 x2+SATA2.0 x4 (PCH)
SATA 3.0 x2(ASM1061)
USB2.0 *12 (Rear*8 Front*4)
USB3.0 *4 (Rear*2 Front*2) co-lay
USB2.0 *4(Rear*2 Front*2)

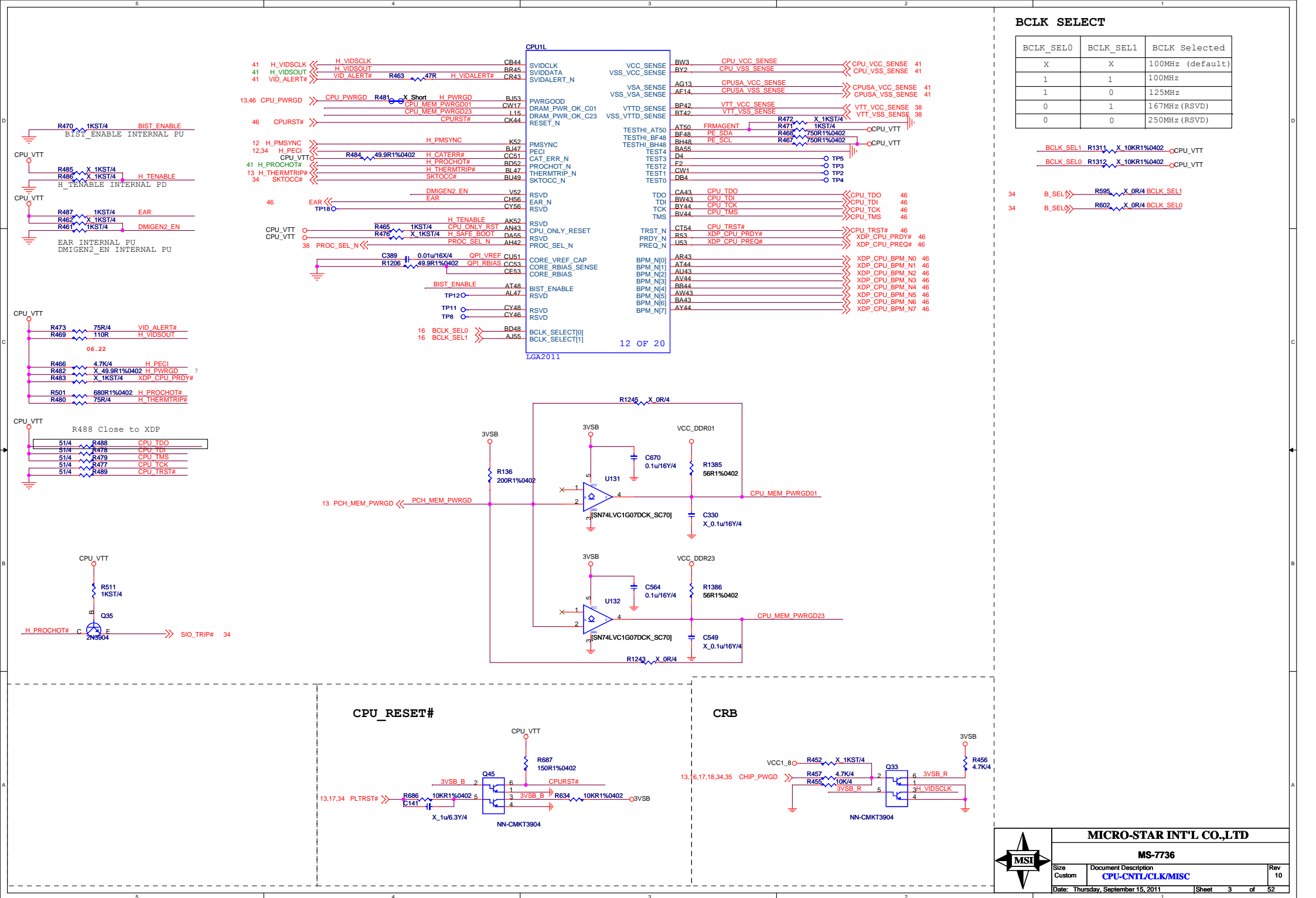
PWM:

CPU:uP1618 (8-Dr.MOS)
CPU_SA:uP1618 (2-Dr.MOS)
CPU_VTT:UP6212 (2-Dr.MOS)
VCC_DDR:UP6212(2-Dr.MOS)
PCH:uP1508 (1-Dr.MOS)

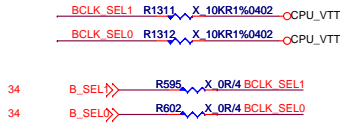
ACPI:


UPI



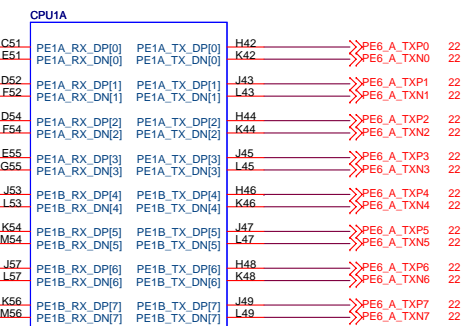
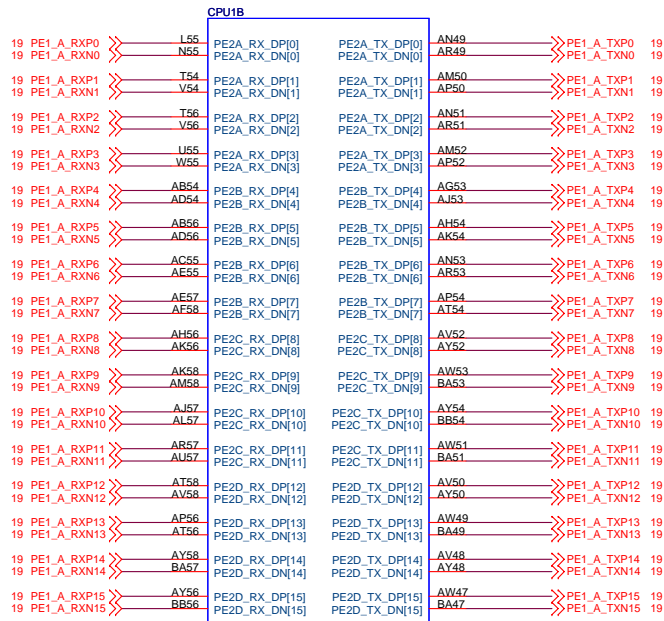


BCLK SELECT		
BCLK_SEL0	BCLK_SEL1	BCLK Selected
X	X	100MHz (default)
1	1	100MHz
1	0	125MHz
0	1	167MHz (RSVD)
0	0	250MHz (RSVD)

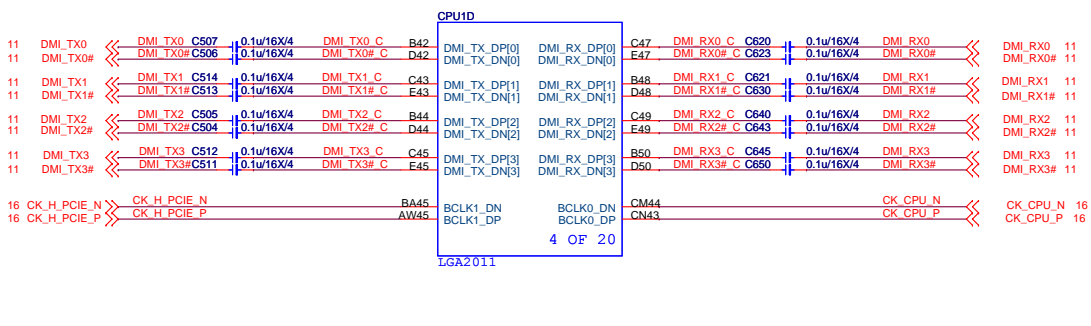
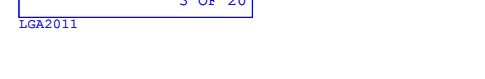
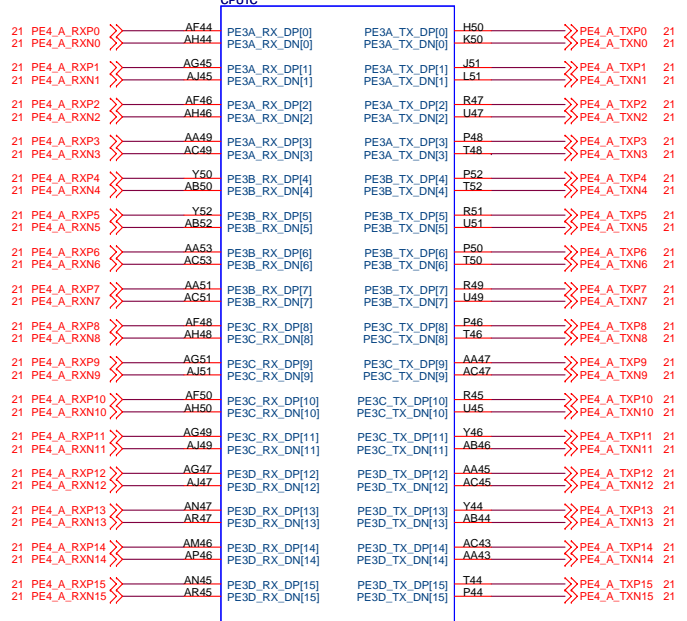




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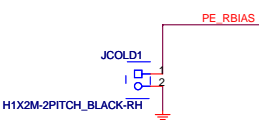



1 OF 20
LGA2011
PE1A : X4 UPLINK
PE1B : X4 SLOT



4 OF 20
LGA2011

Reserve for Cold Bug





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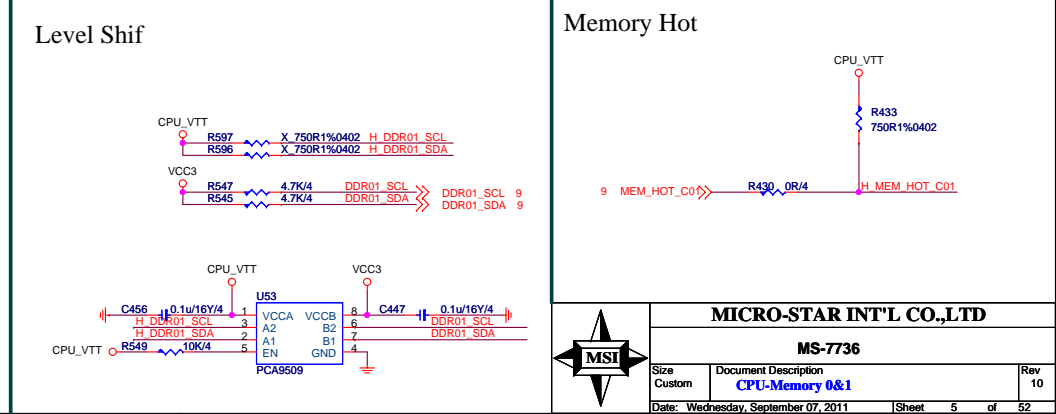
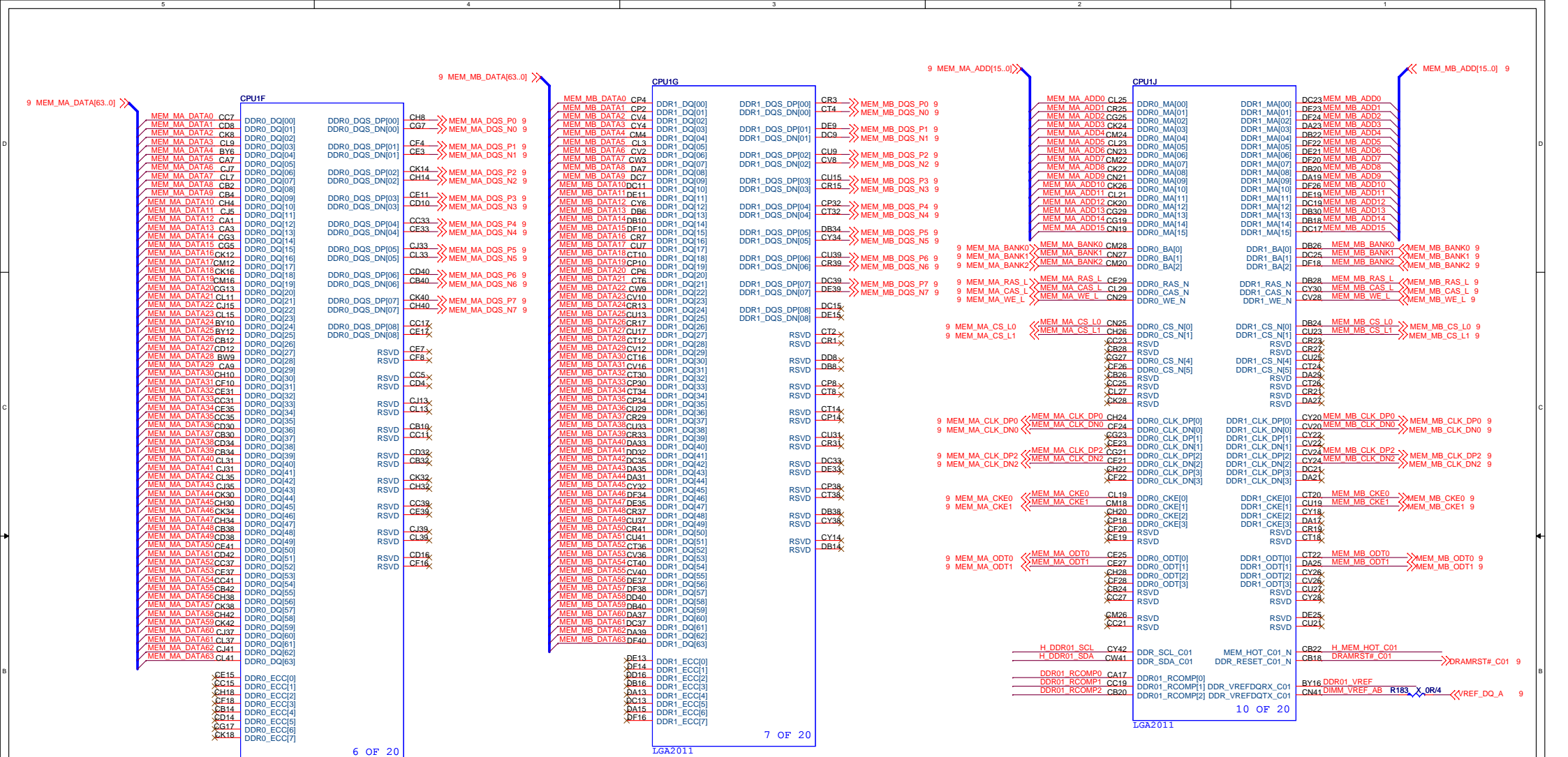
MS-7736

Size Custom Document Description CPU-PEG/DMI

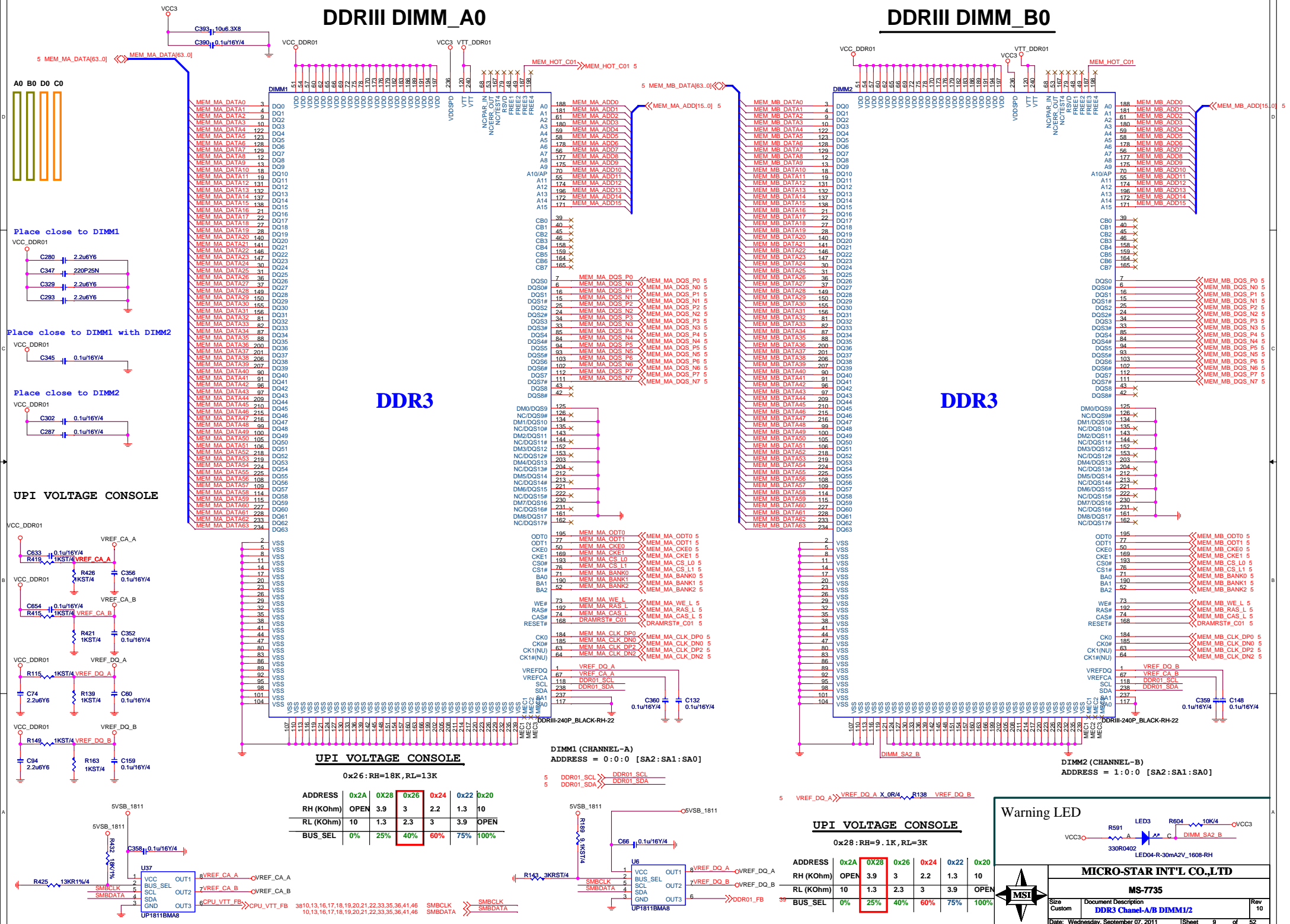
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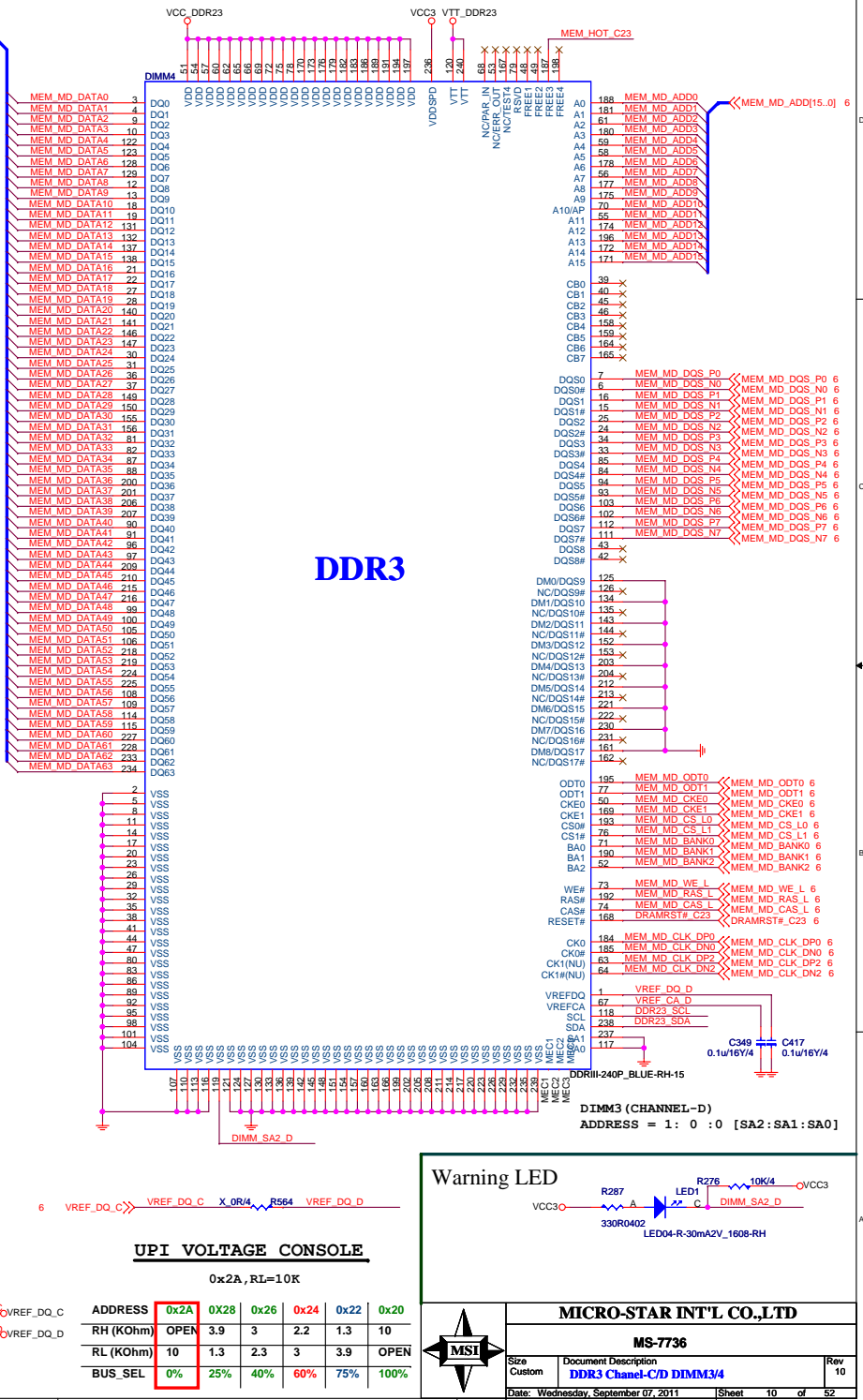
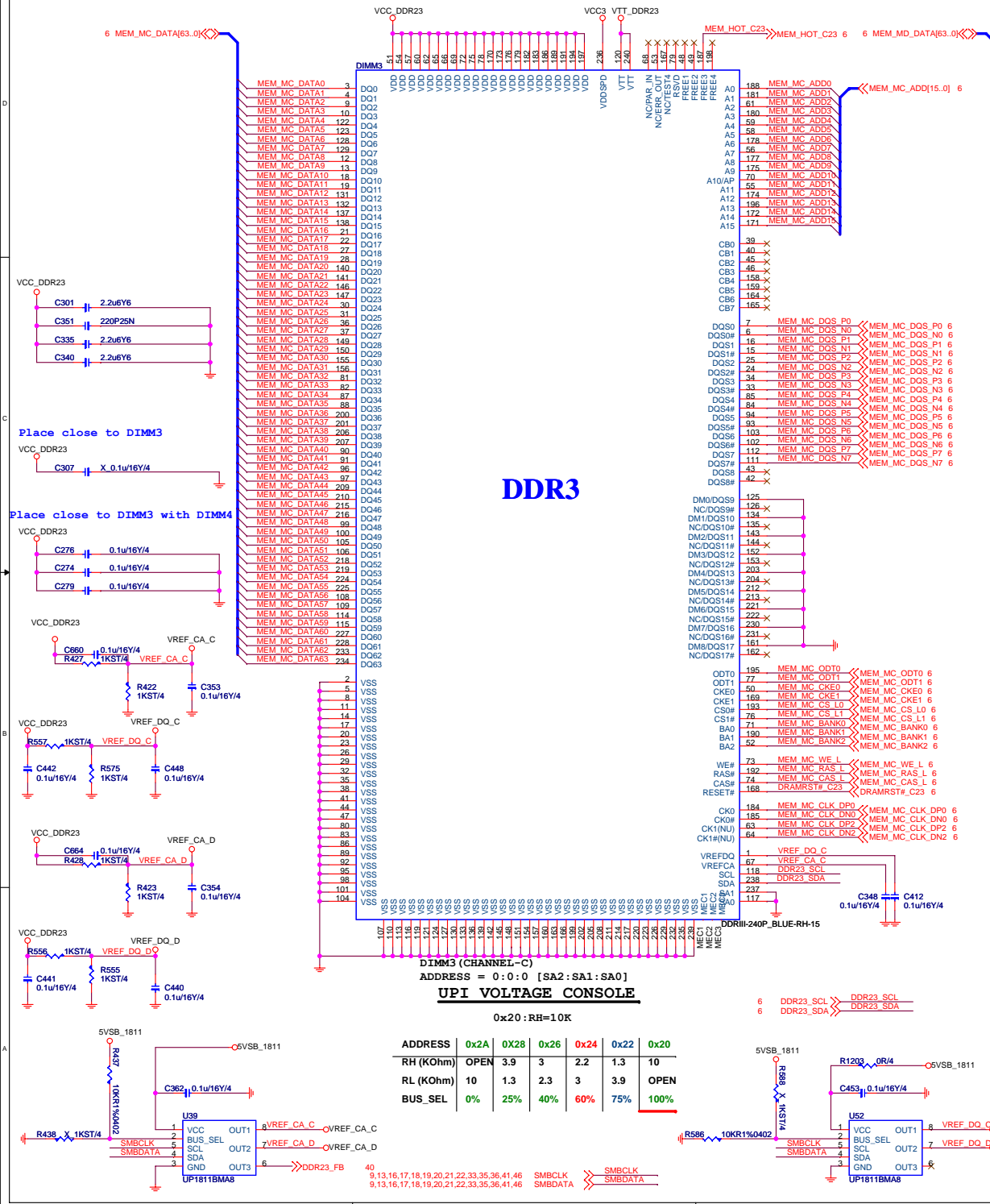


DDRIII DIMM_B0



DDR3 DIMM_C0

DDR3 DIMM_D0



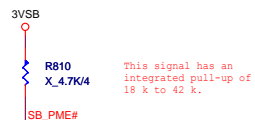
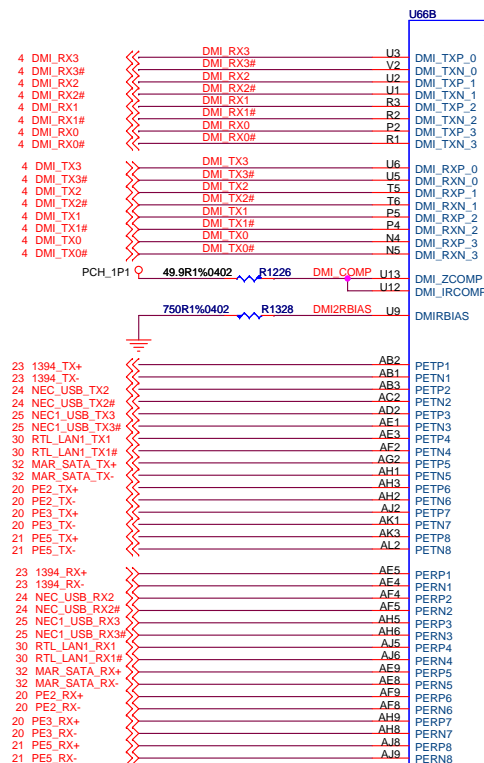
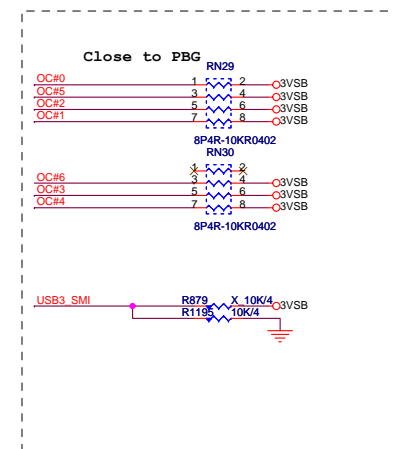


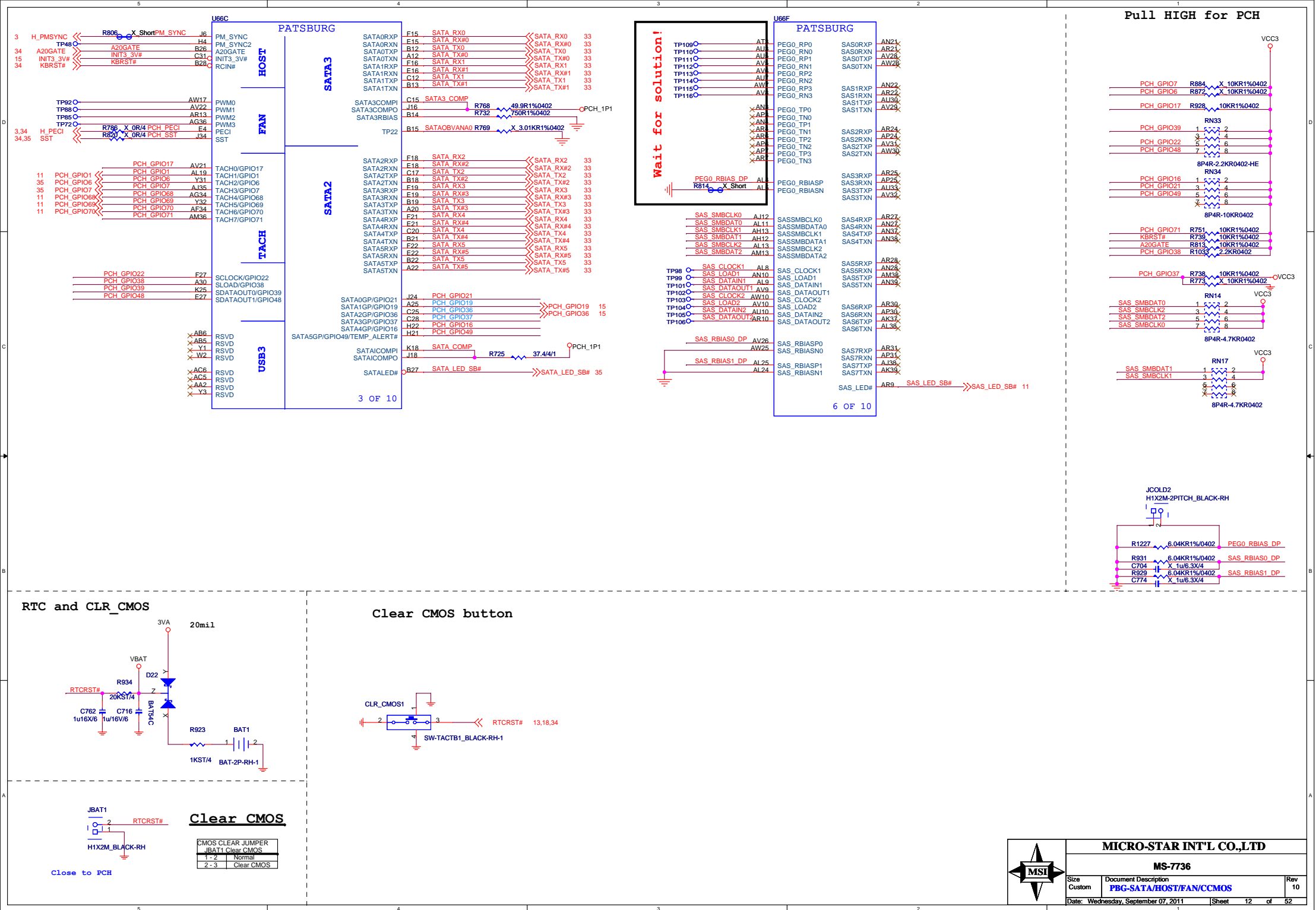
Figure 10 shows the pin connections for the 8P4R-8.2KR0402 module. The module has four pin headers: RN19, RN20, RN32, and RN18. Each header has 8 pins. The connections are as follows:

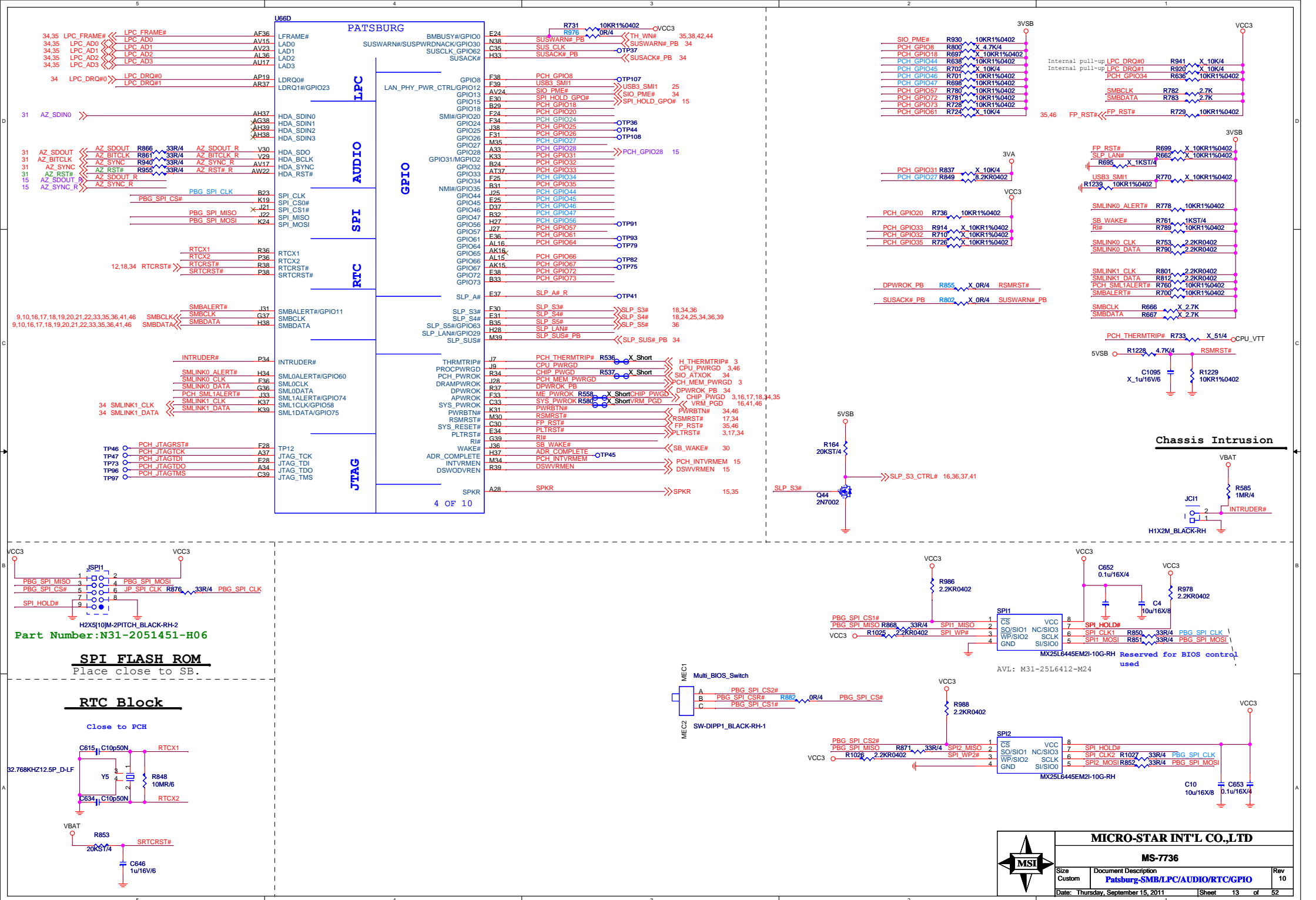
- Header RN19:**
 - Pin 1: VCC3
 - Pin 2: PSFT_ON#
 - Pin 3: NSFT_ON#
 - Pin 4: PERR#
 - Pin 5: PIROA#
 - Pin 6: PCH_GPIO69
 - Pin 7: PIROG#
 - Pin 8: Ground
- Header RN20:**
 - Pin 1: VCC3
 - Pin 2: SAS_LED_SB#
 - Pin 3: TRDY#
 - Pin 4: LOOK#
 - Pin 5: PCH_GPIO1
 - Pin 6: Ground
 - Pin 7: Ground
 - Pin 8: Ground
- Header RN32:**
 - Pin 1: VCC3
 - Pin 2: SERR#
 - Pin 3: PIROD#
 - Pin 4: PIROH#
 - Pin 5: IRDY#
 - Pin 6: Ground
 - Pin 7: Ground
 - Pin 8: Ground
- Header RN18:**
 - Pin 1: VCC3
 - Pin 2: PIROB#
 - Pin 3: STO#
 - Pin 4: PIROC#
 - Pin 5: Ground
 - Pin 6: Ground
 - Pin 7: Ground
 - Pin 8: Ground

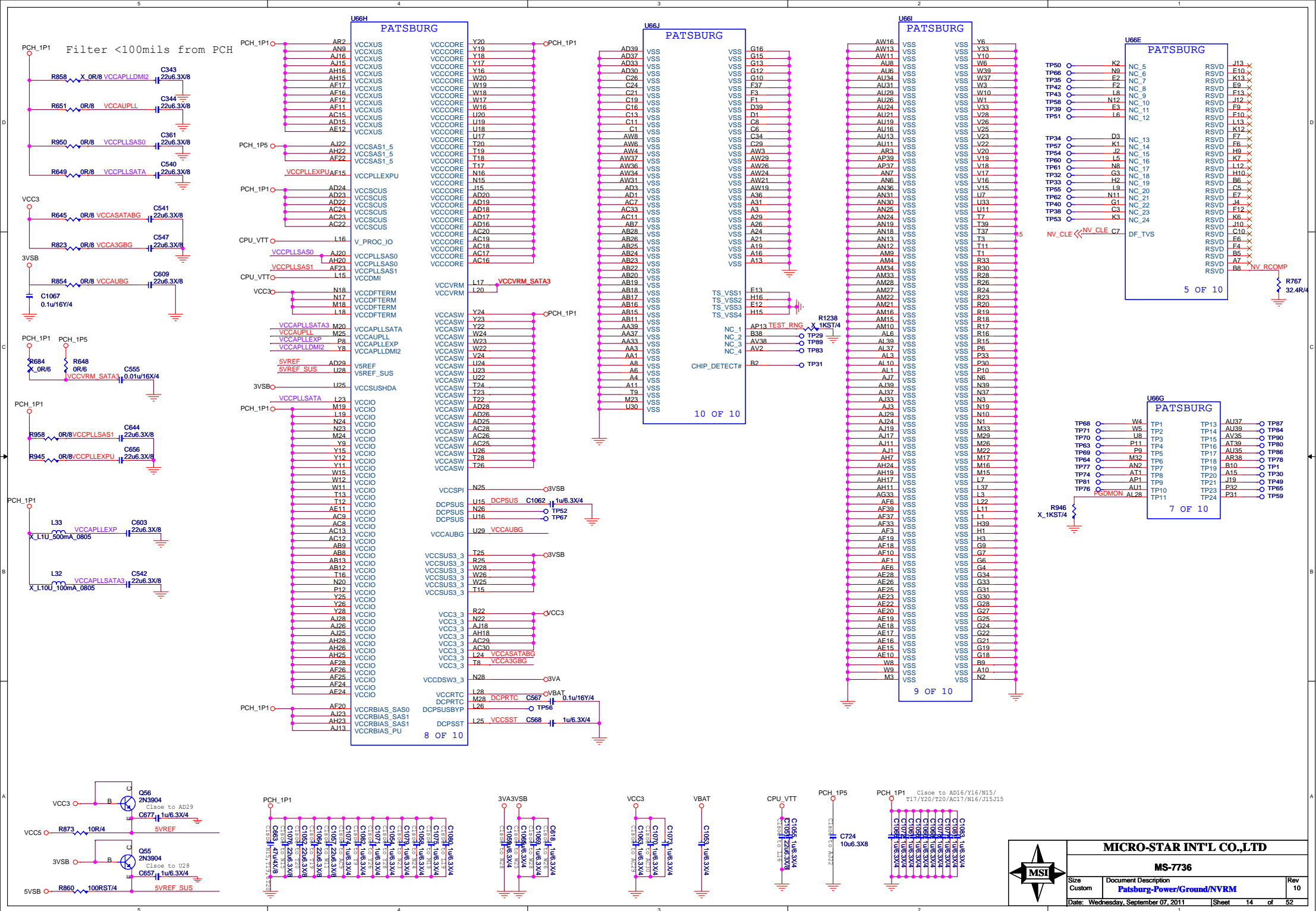
The module is connected to a 5V supply (VCC3) and ground. The signals are connected to the module pins as follows:

- PSFT_ON# (pin 2, RN19)
- NSFT_ON# (pin 3, RN19)
- PERR# (pin 4, RN19)
- PIROA# (pin 5, RN19)
- PCH_GPIO69 (pin 6, RN19)
- PIROG# (pin 7, RN19)
- SAS_LED_SB# (pin 2, RN20)
- TRDY# (pin 3, RN20)
- LOOK# (pin 4, RN20)
- PCH_GPIO1 (pin 5, RN20)
- SERR# (pin 2, RN32)
- PIROD# (pin 3, RN32)
- PIROH# (pin 4, RN32)
- IRDY# (pin 5, RN32)
- PREQ#0 (pin 2, RN18)
- SERIRQ (pin 3, RN18)
- PREQ#1 (pin 4, RN18)
- PREQ#2 (pin 5, RN18)
- PREQ#3 (pin 6, RN18)
- DEVSEL# (pin 7, RN18)
- PIROB# (pin 2, RN18)
- STO# (pin 3, RN18)
- PIROC# (pin 4, RN18)
- PCH_GPIO70 (pin 2, RN18)
- FRAME# (pin 3, RN18)



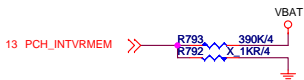
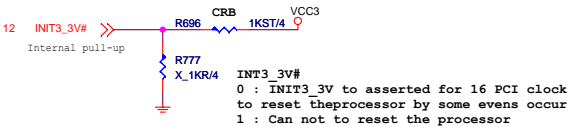
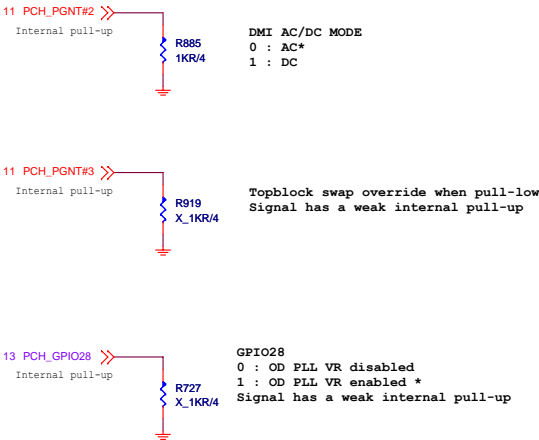
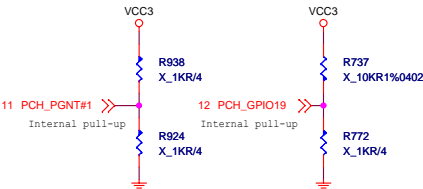






PCH Straps

BOOT DEVICE	GNT1	SATA1GP/GPIO19
LPC	0	0
PCI	1	0
SPI	1	1

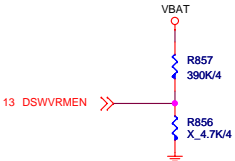


INTVRMEN

0 : DISABLE INTERNAL VRM

1 : ENABLE INTERNAL VRM *

When these voltage regulators are enabled, the integrated GbE only operates at 10/100 Mbps during S3-S5.

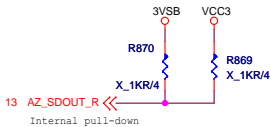


DSWVRMEN

0 : Disable Internal Deep Sleep 1.05 V regulators.

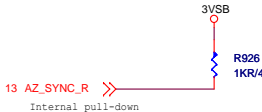
1 : Enable Internal Deep Sleep 1.05 V regulators.

This signal enables the internal Deep Sleep 1.05 V regulators. Must beconnected even when not supporting DSW.



HDA_SDO

Disable ME in Manufacturing Mode when pull LOW ????

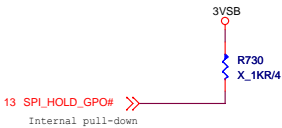


HDA_SYNC

OD PLL VR SUPPLY SEL

0 : 1.8V SUPPLY

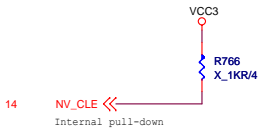
1 : 1.5V SUPPLY *



GPIO15

0 : TLS CIPHER SUITE WITH NO CONFIDENTIALITY *

1 : TLS CIPHER SUITE WITH CONFIDENTIALITY

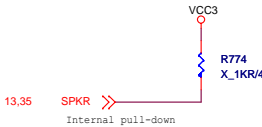


DMI/FDI TERMINATION VOLTAGE

DC COUPLED: TX/RX TO VCC ISF SAMPLED HIGH

DC COUPLED: TX/RX TO VSS IF SAMPLED LOW *?

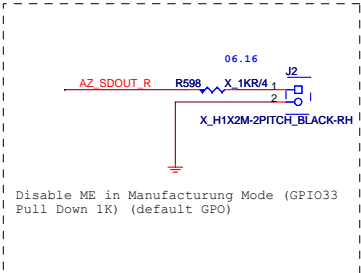
AC COUPLED: TX SET TO VCC/2, RX SET TO VSS REGARDLESS OF THIS STRAP



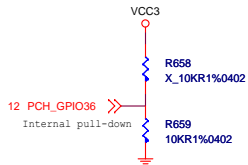
SPKR

0 : EN TCO REBOOT *

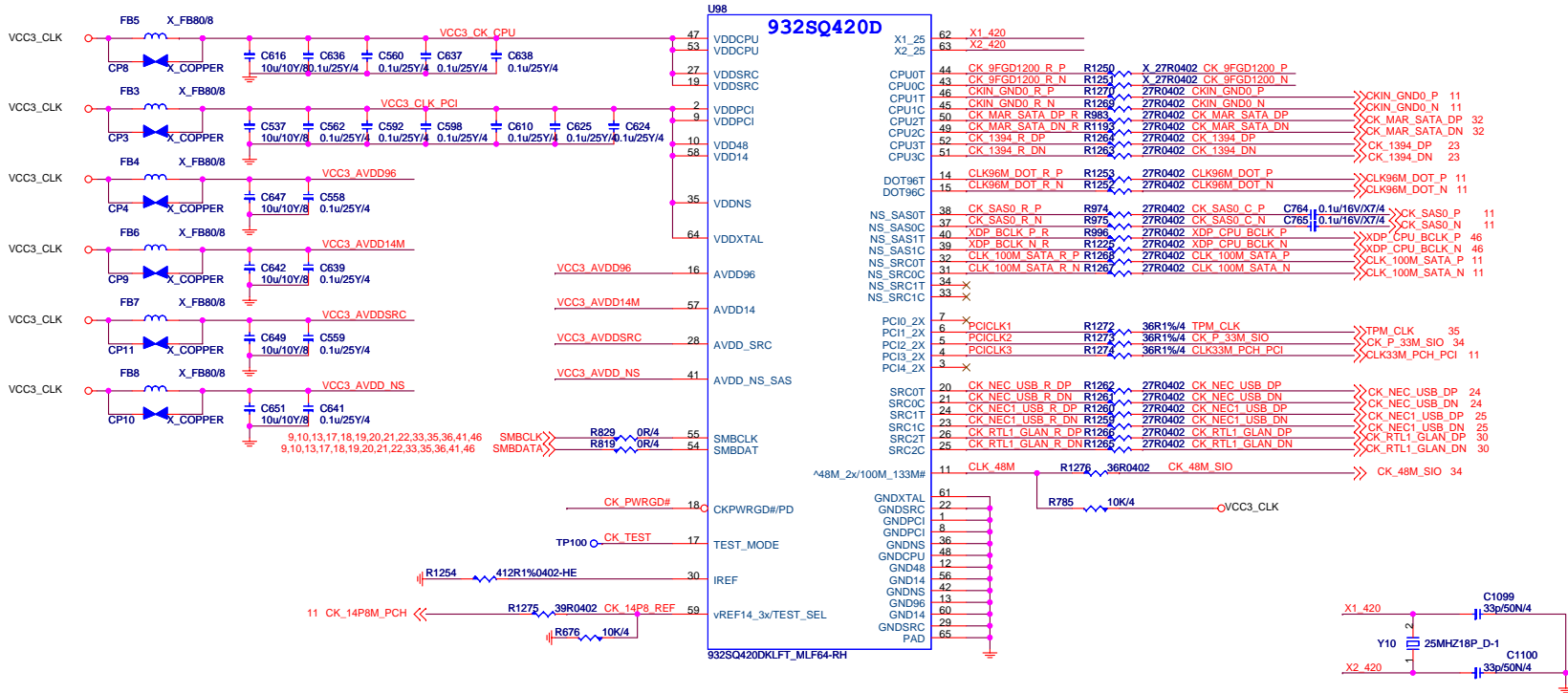
1 : DIS TCO REBOOT



Disable ME in Manufacturing Mode (GPIO33 Pull Down 1K) (default GPO)

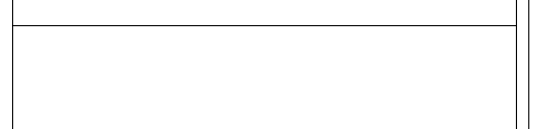
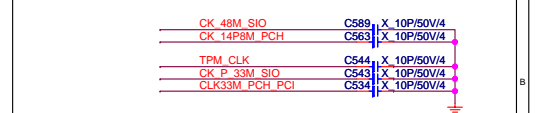
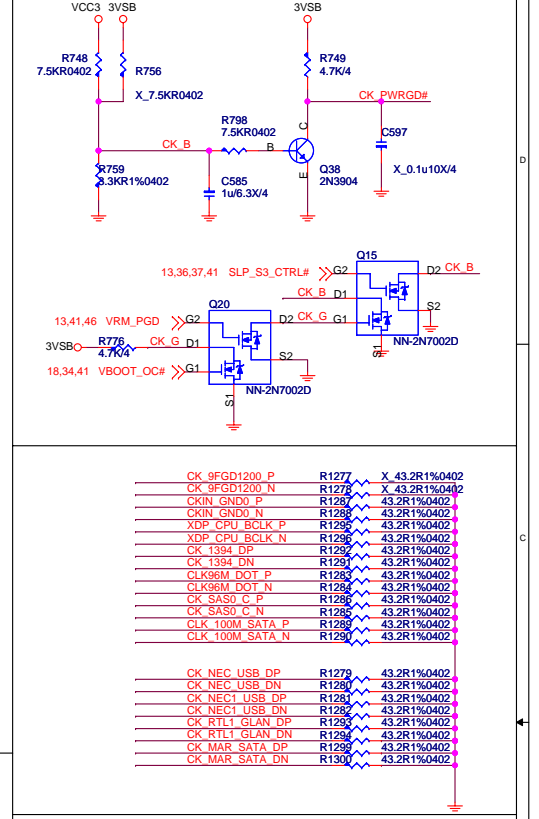
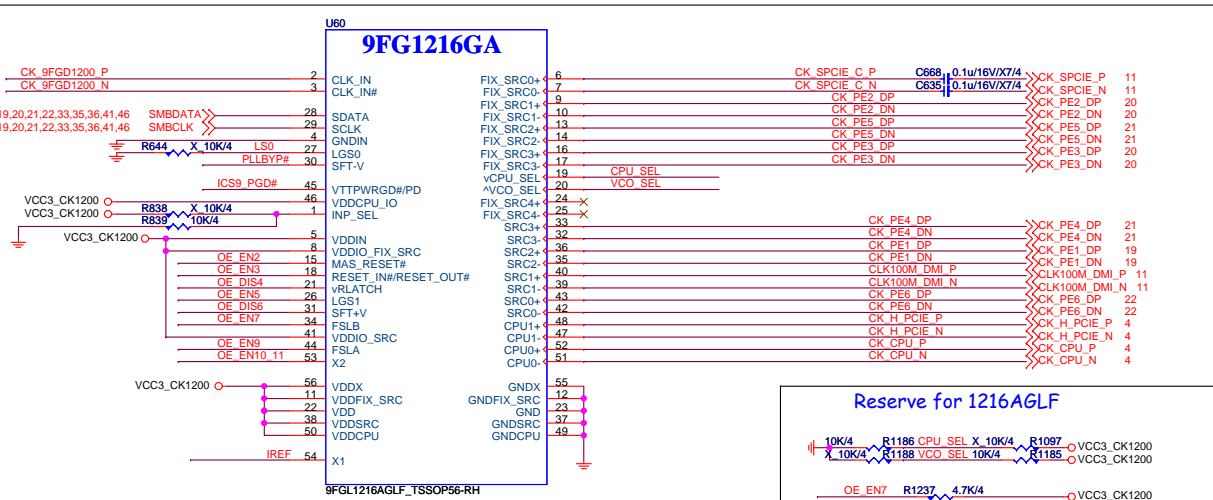
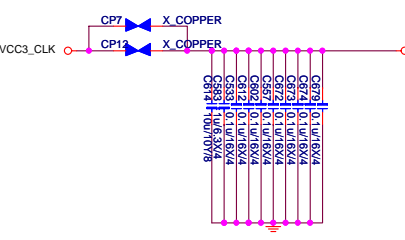


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MS-7736		
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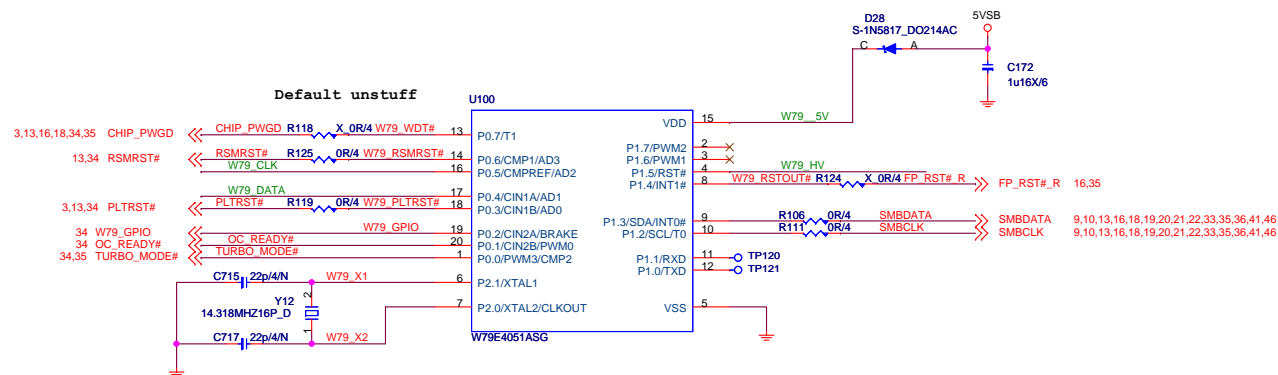


9FGD1200D-5 Colay with 9FG1216AG

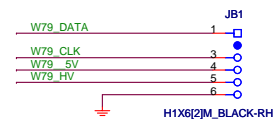
PIN#	9FGD1200D-5	9FG1216AG
1	HIGH_BW	INP_SEL
4	SMB_A0	GNDIN
5	OE0#	VDDIN
8	OE1#	VDDIO_FIX_SRC
15	OE#2	MAS_RESET#
18	OE3#	RESET_IN#/RESET_OUT#
19	DIF_4	CPU_SEL
20	DIF_4#	VCO_SEL
21	OE4#	RELATCH
24	DIF_5	SRC4+
25	DIF_5#	SRC4-
26	OE5#	LGSPARE1
27	SMB_A1	LGSPARE0
30	SMB_A2_PLLBYP#	SFT-v
31	OE6#	SFT+v
34	OE7#	FSLB
41	OE8#	VDDIO_SRC
44	OE9#	FSLA
46	VFS_CA_410	VCCDCPU_IO
53	OE10_11#	X1
54	IREF	X2



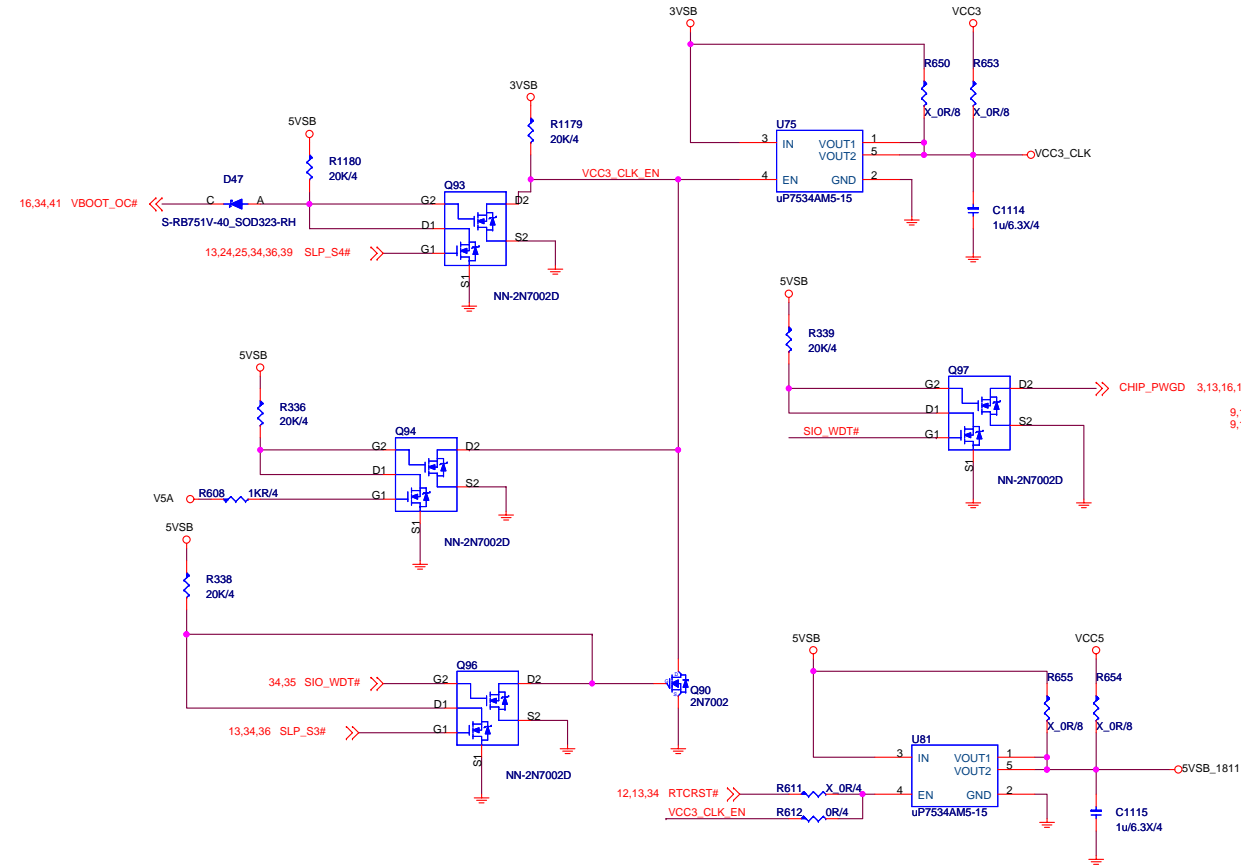
out for Full reset, can pull up to 3V
RSMRST# for 8051 refer to read GPIO state
ICP Programmer
ICP Programmer
PLTRST# is a power on event for 8051
Reserved, can pull to 3V
BIOS inform to 8051 the OC ready, can pull up to 3V
OC Button, can pull up to 3V



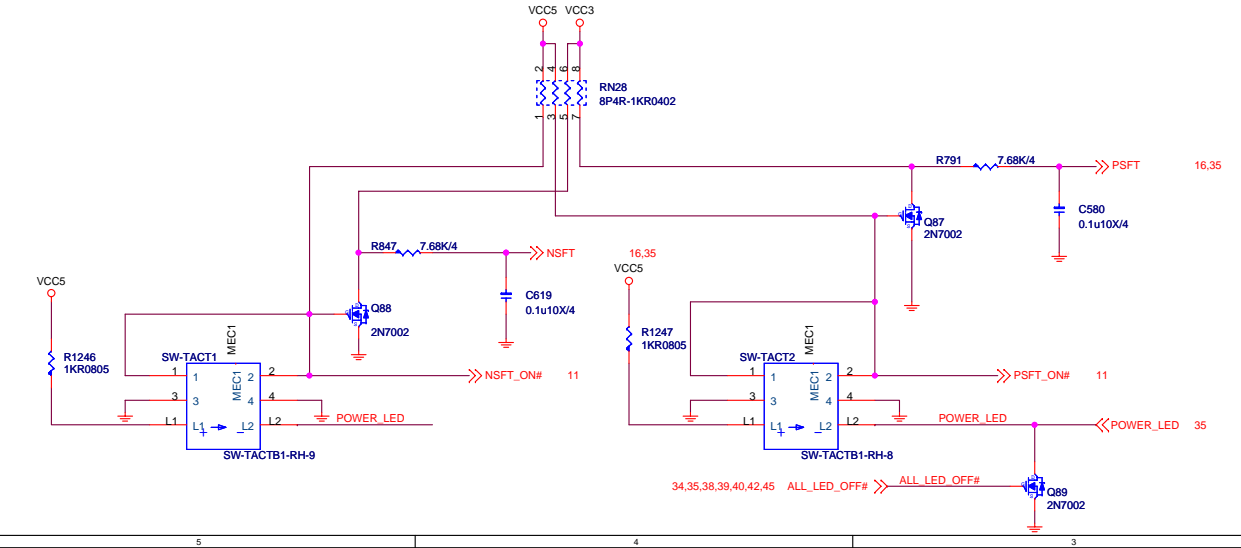
緒魁CONNECT



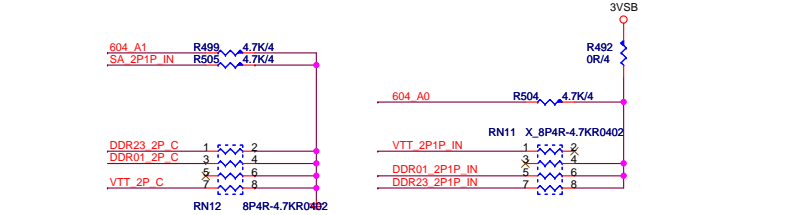
POWER METER



+-續圖

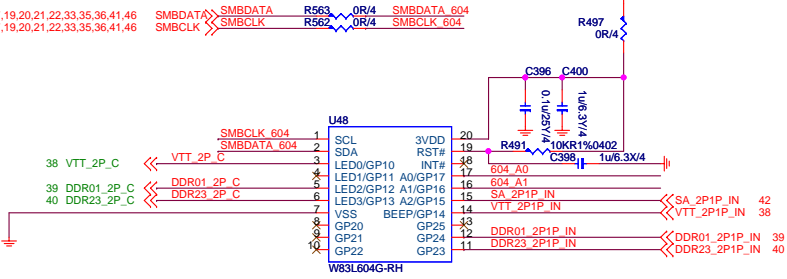


GPIO Controller - B LED / VTT / PHASE6

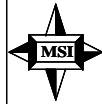


Programming
Default GP1 ==>GP0 (O/D) ==>GP0 (O) ==>GP0 (O) 1

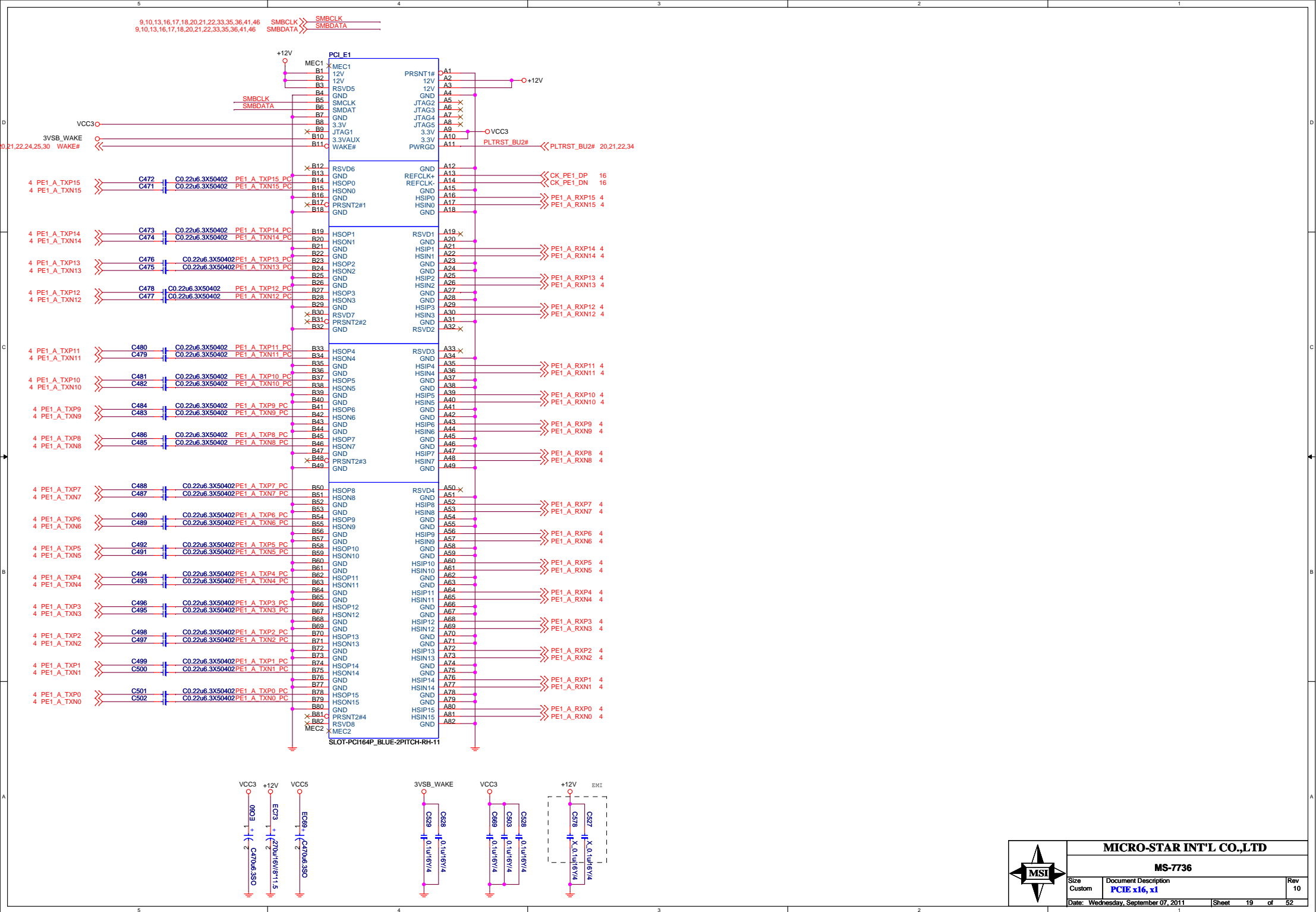
SMBus Address 0X32



Only VTT_PSI_GP0# Default High
Others Default Low



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Custom	41.OC SWITCH/W604GPIO CTL/OC	0A
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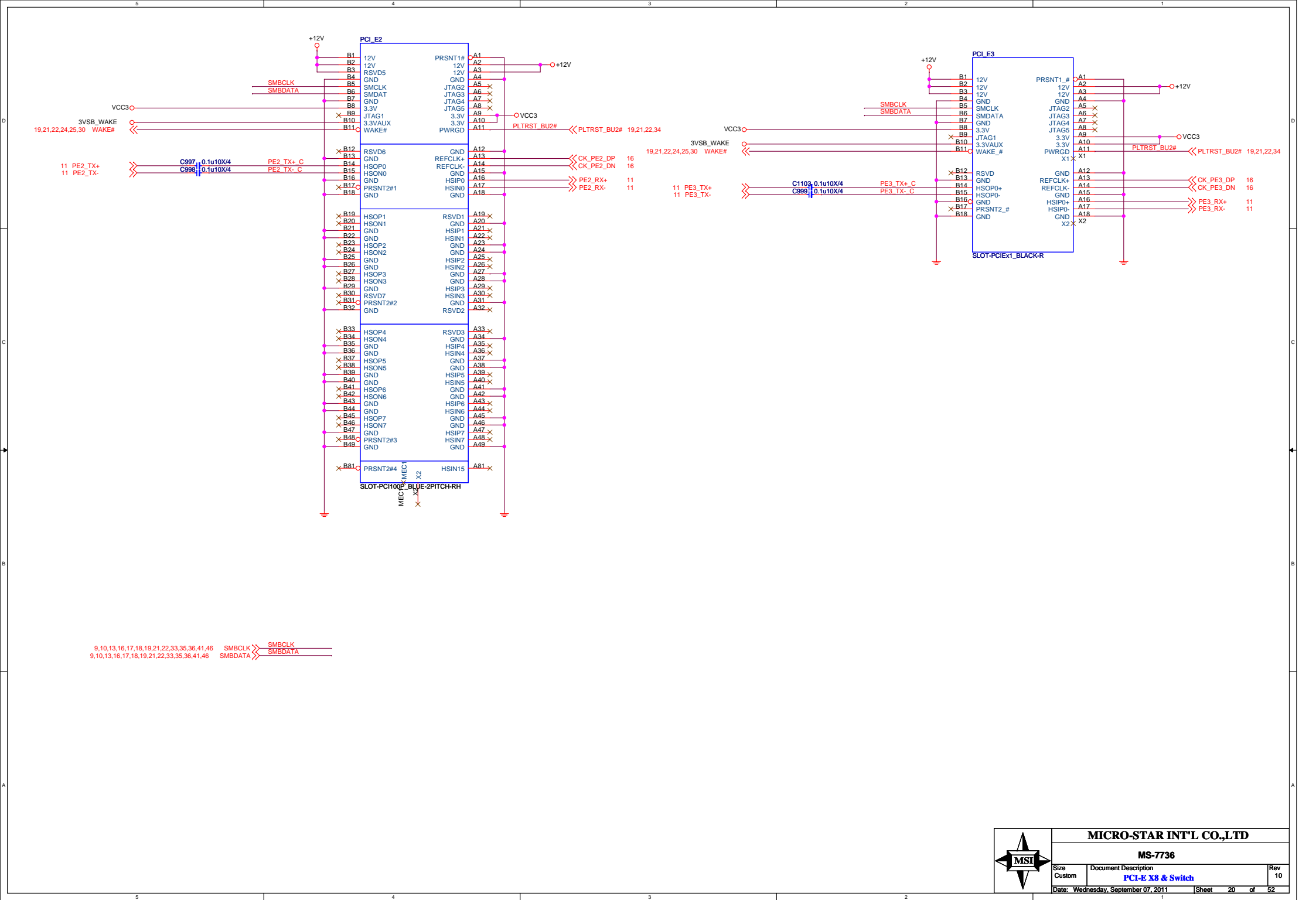
Size
Custom

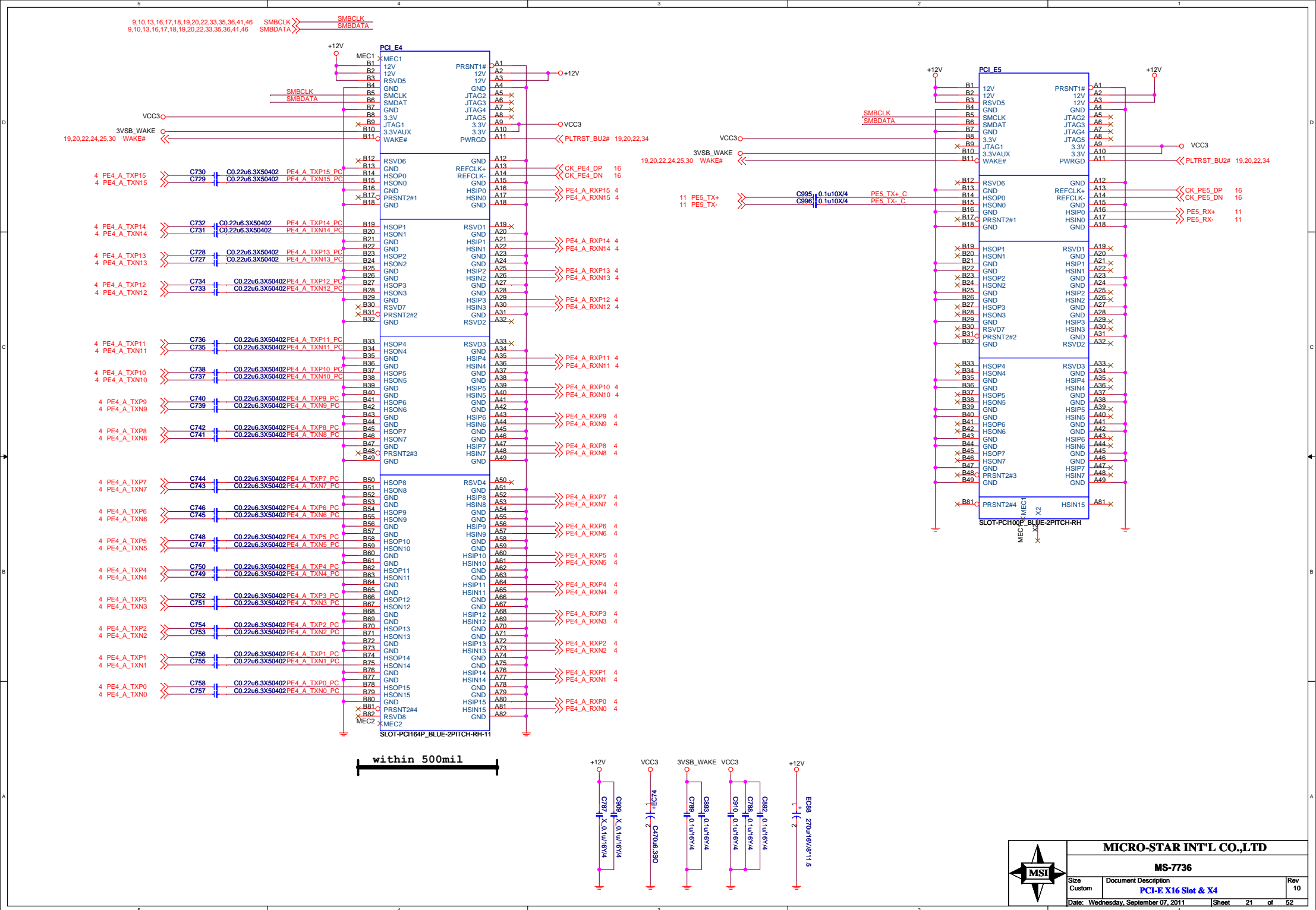
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PCIE x16, x1

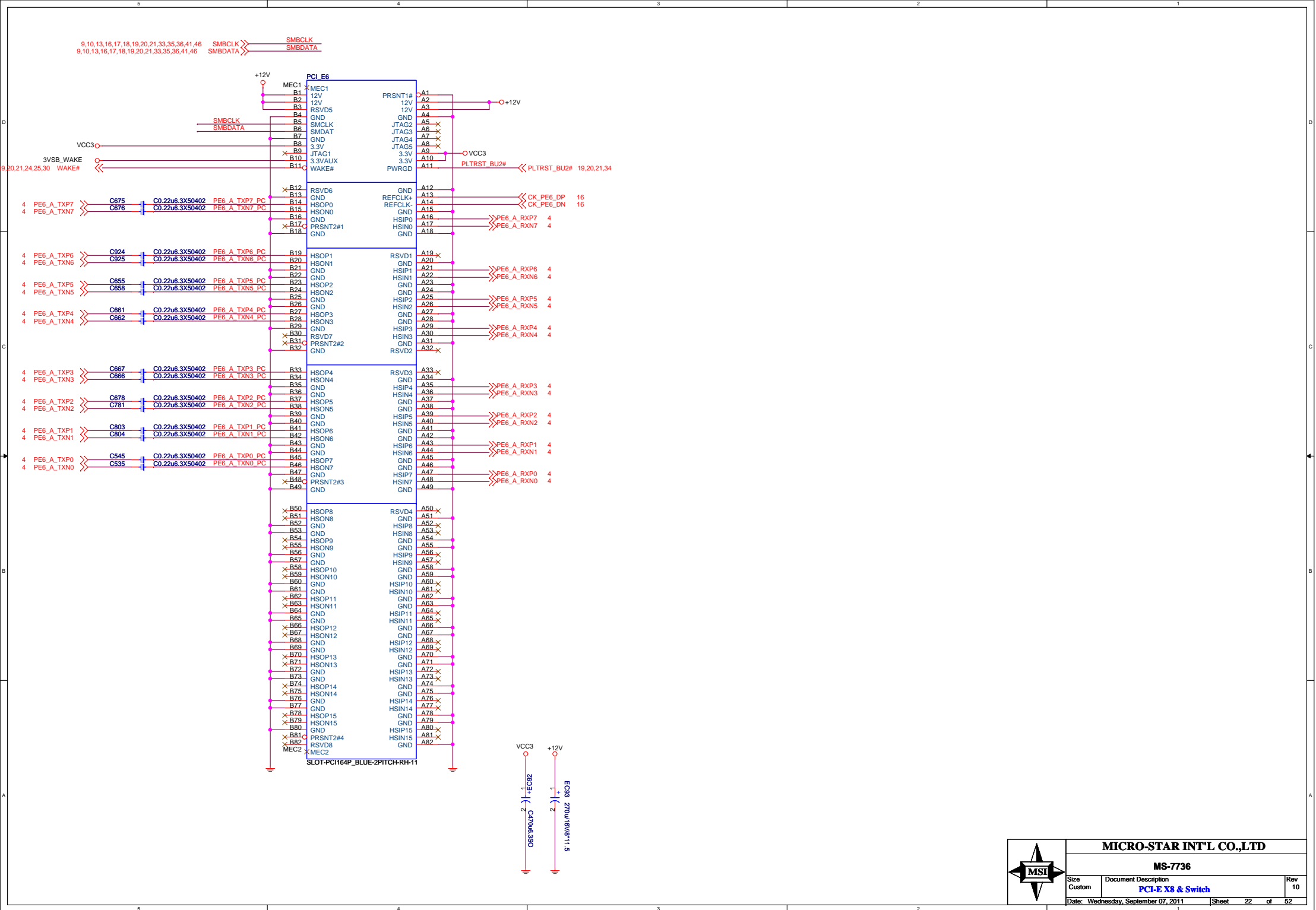
Rev	
10	

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[illegible]

EE PROM

U74
HT24LC02-8 SOP-A-RH

Rear 1394 port

Place near VIA_6135

Front 1394 pin header

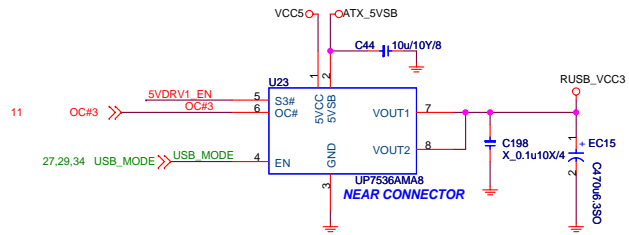
Place near VIA_6135

For Intel 1394 pinheader

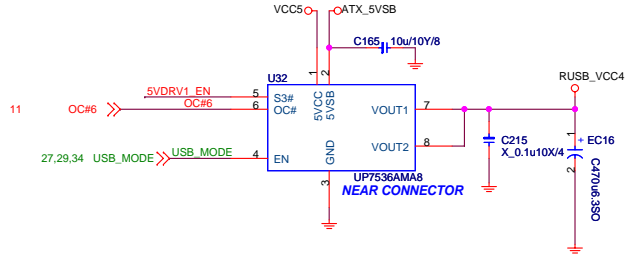
	MICRO-STAR INT'L CO.,LTD	
	MS-7736	
	Size Custom Document Description VT6315N-1394	Rev 10

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USB POWER FOR PORT 10,11

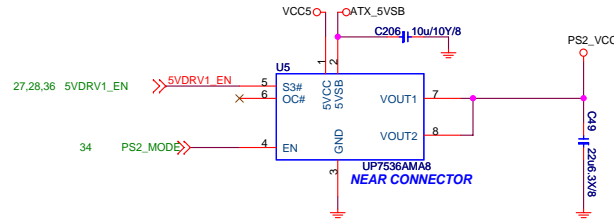


USB POWER FOR PORT 10,11

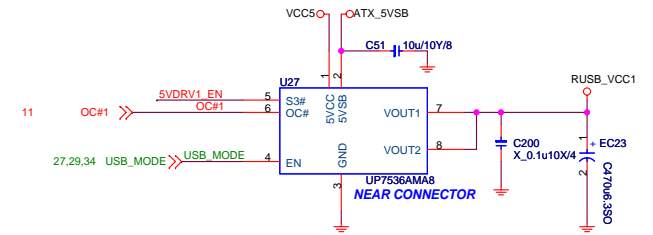


Rear USB Connector

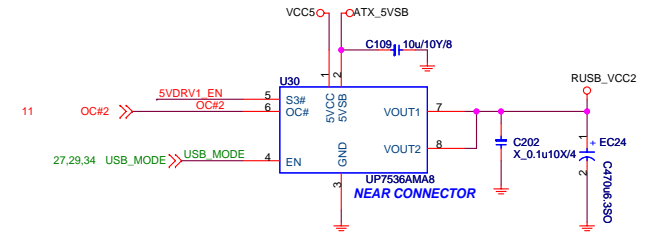
PS2 POWER



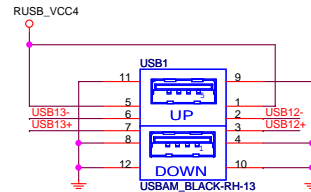
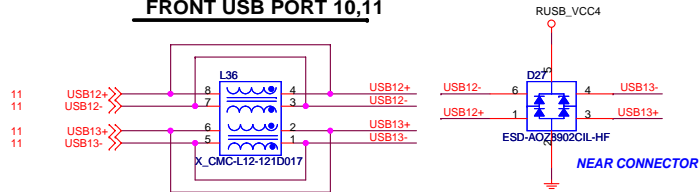
USB POWER FOR PORT 10,11



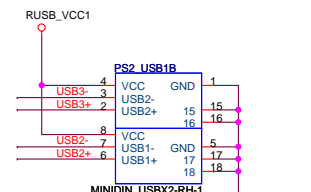
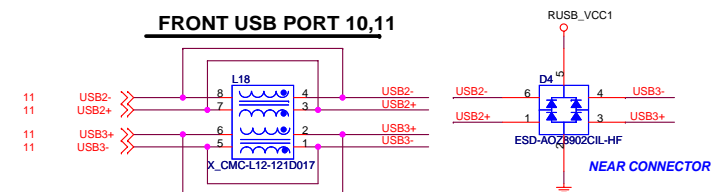
USB POWER FOR PORT 10,11



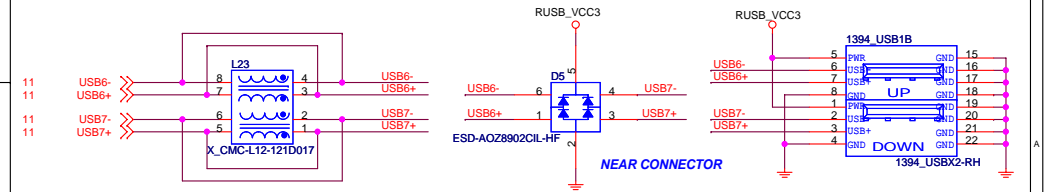
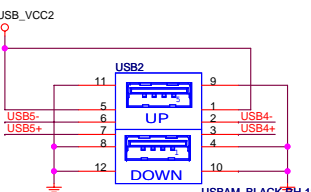
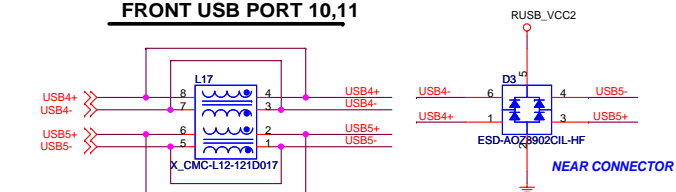
FRONT USB PORT 10,11




FRONT USB PORT 10,11

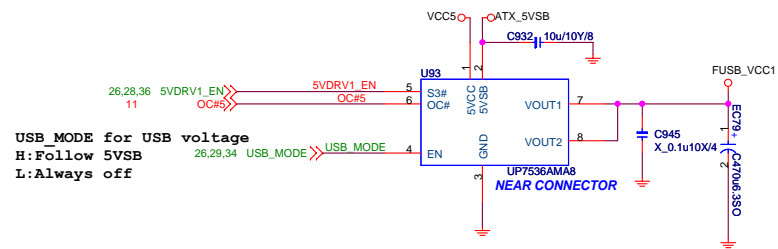


FRONT USB PORT 10,11

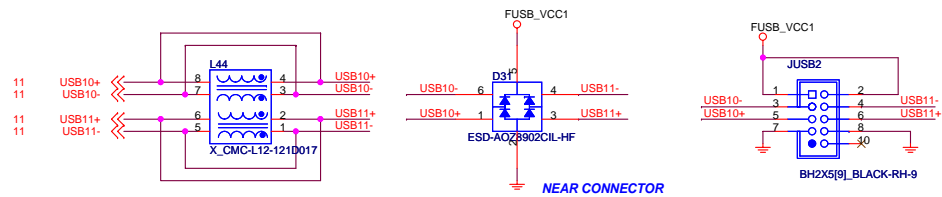


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USB POWER Front PORT 2,3



FRONT USB PORT 2,3

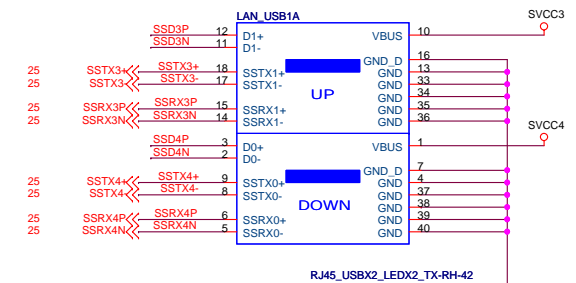
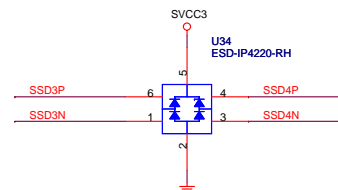
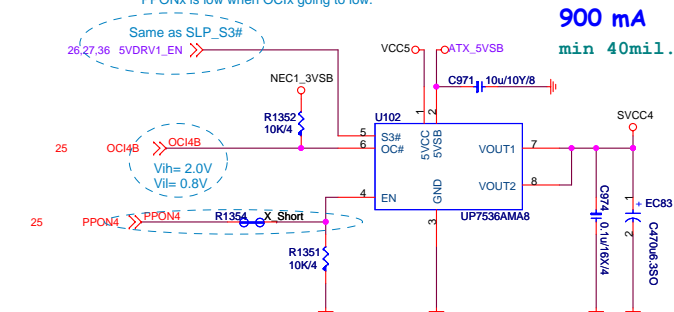
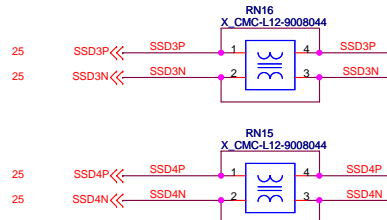
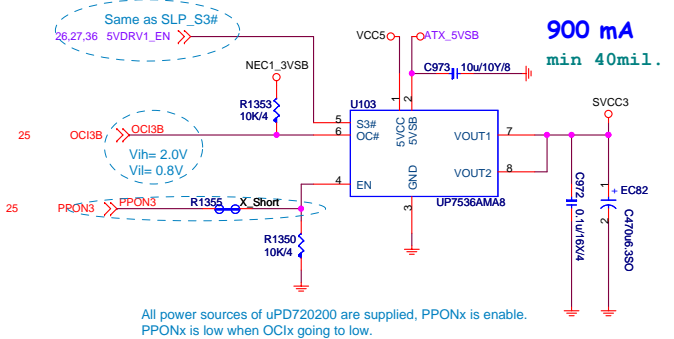
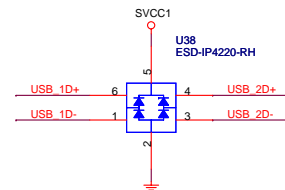
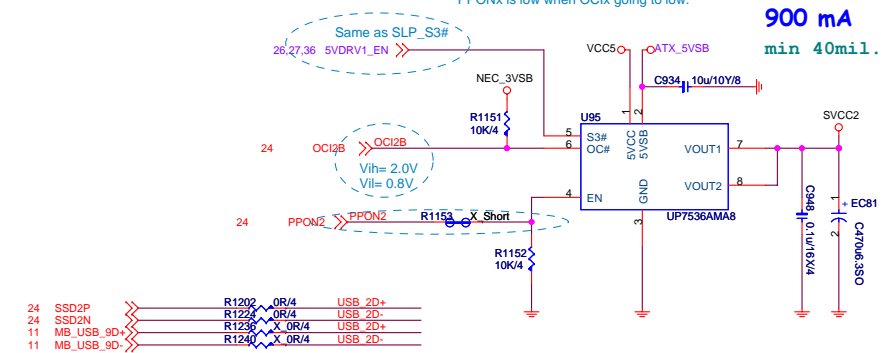
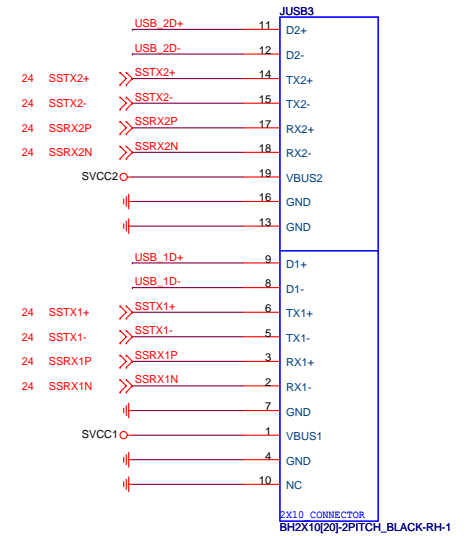
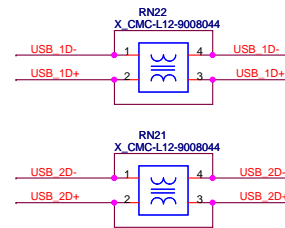
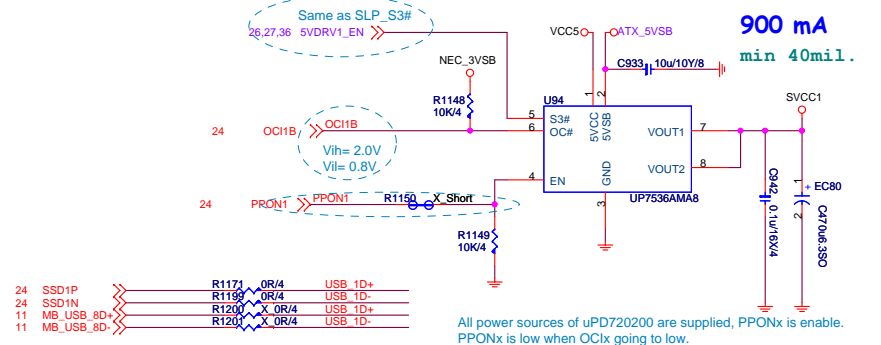


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FRONT USB PORT 4,5

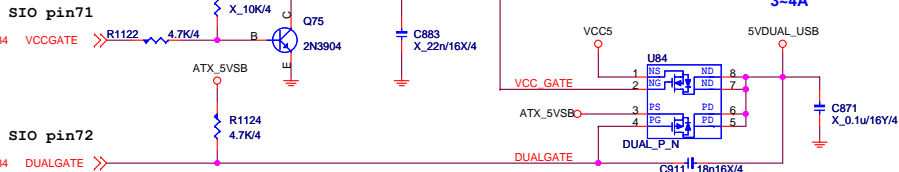


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5VDUAL_USB



SIO GPIO40 Pin7 (I VSB3V)

USB_CHARGE: (OD)

```
0: Don't support USB charge and resume.
1: Support USB charge and resume.
```

Power plug in , H/W default support USB charge.

Pin power	I_3VSB or VBAT
Register power	I_3VSB or VBAT
Register reset	I_3VSB or VBAT

SIO GPIO40

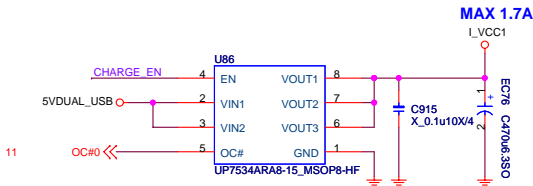


```
Pin power      I_3VSB
Register power  I_3VSB
Register reset  I_3VSB
```

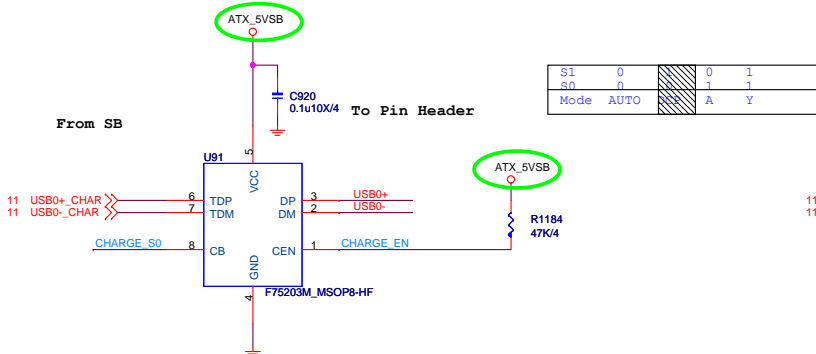
Update~2010.9.15



USB POWER PORT 0 For USB Charging

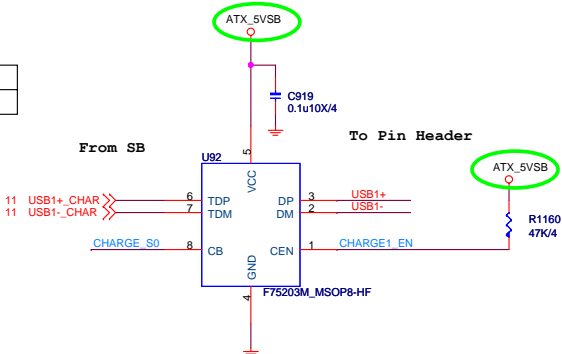
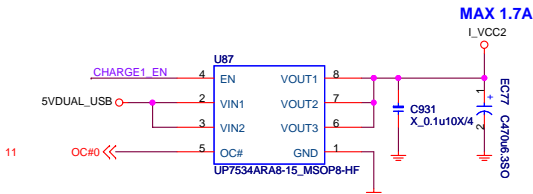


**** If your spec will not need bom option, please don't co-lay blue labels.**

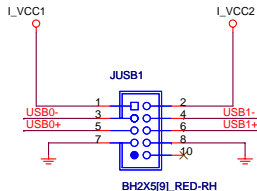
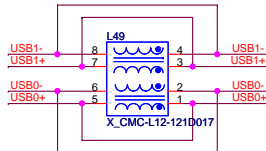


A type
2.70V< D+ <3.1 V
1.85V< D- < 2.1V
For i-Pad / i-Phone 4G charges current up to 1.6A.

USB POWER PORT 1 For USB Charging



FRONT USB PORT 0,1



Please name the pin header JUSB1 and use SB USB0,1 link for charger port.

PI5USB14550 has internal EDS diode.

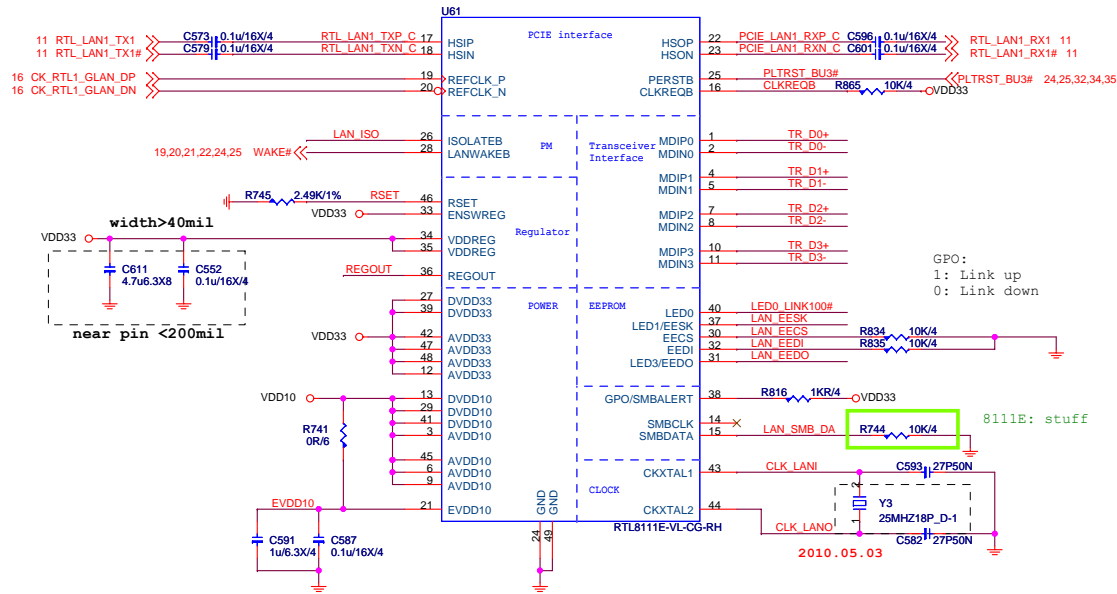


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RTL8111E Giga LAN

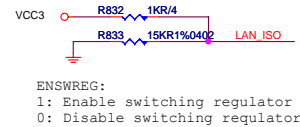
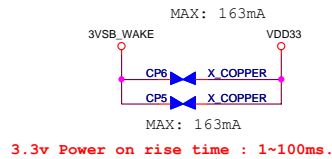


Pin49: 9 via from top layer to GND layer and make the via at the center of IC.

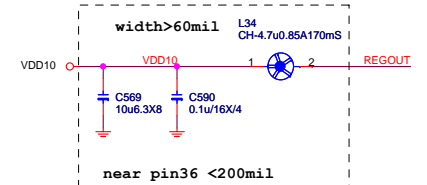
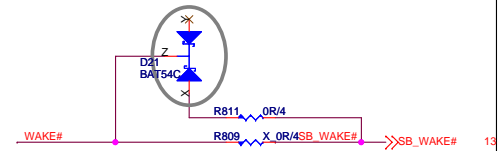
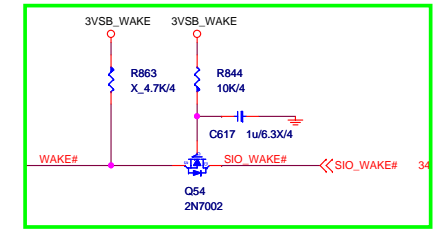
only support LED0+LED1/LED1+LED3 dual color LED combinations when using EEPROM

8111E POWER Consumption

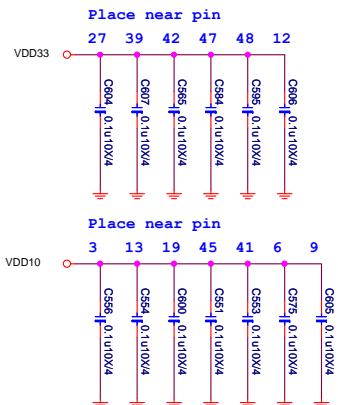
	3.3V	mW
10 M Idle/TxRx	12/66	40/218
100 M Idle/TxRx	31/44	102/145
Giga Idle/TxRx	135/163	452/538
ALDPS	4	13



LAN/PCIE/PCI Wake Up CTRL Circuit



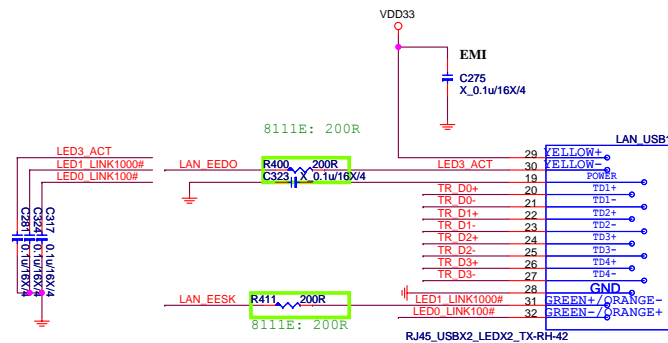
CHOKE (>0.6A) AVL:
L04-22A7470-T04
*L04-47A7340-T04
L04-47A7330-T04
L04-47A7320-T04



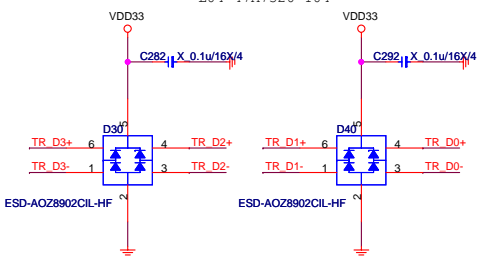
Giga-Lan	10/100-Lan
N58-22F0731	N58-22F0771
Link Yellow	Link Yellow
Active Blinking	Active Blinking
1000 Orange	100 Green
100 Green	10 None
10 None	
19 Yellow	19 Yellow
21 Orange	21 Green
22 Green	22 Green

only support LED0+LED1/LED1+LED3 dual color LED combinations when using EEPROM

LAN Connector

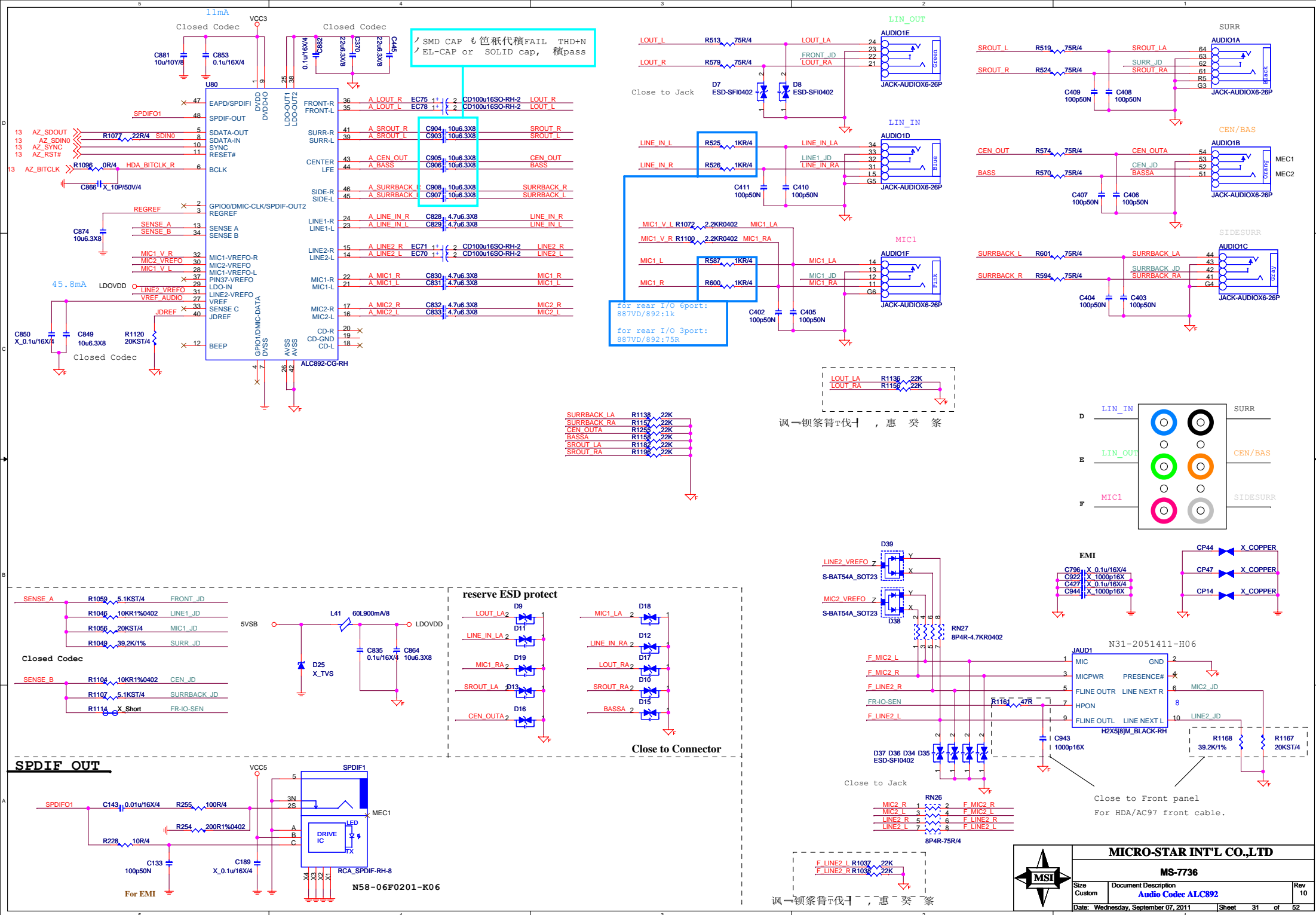


AVL:
N58-22F0731-I60
N58-22F0731-S42
N58-22F0731-U30

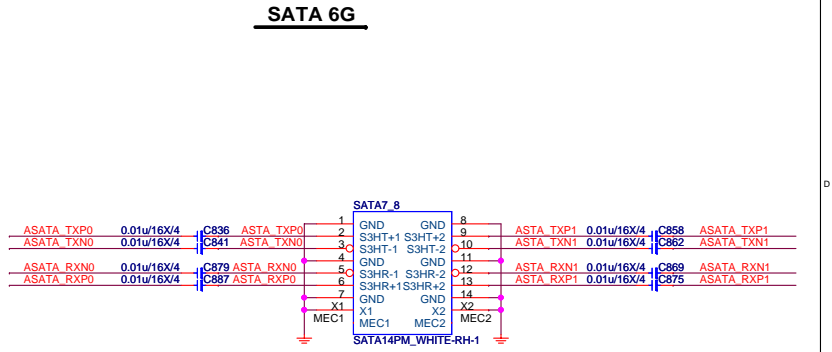
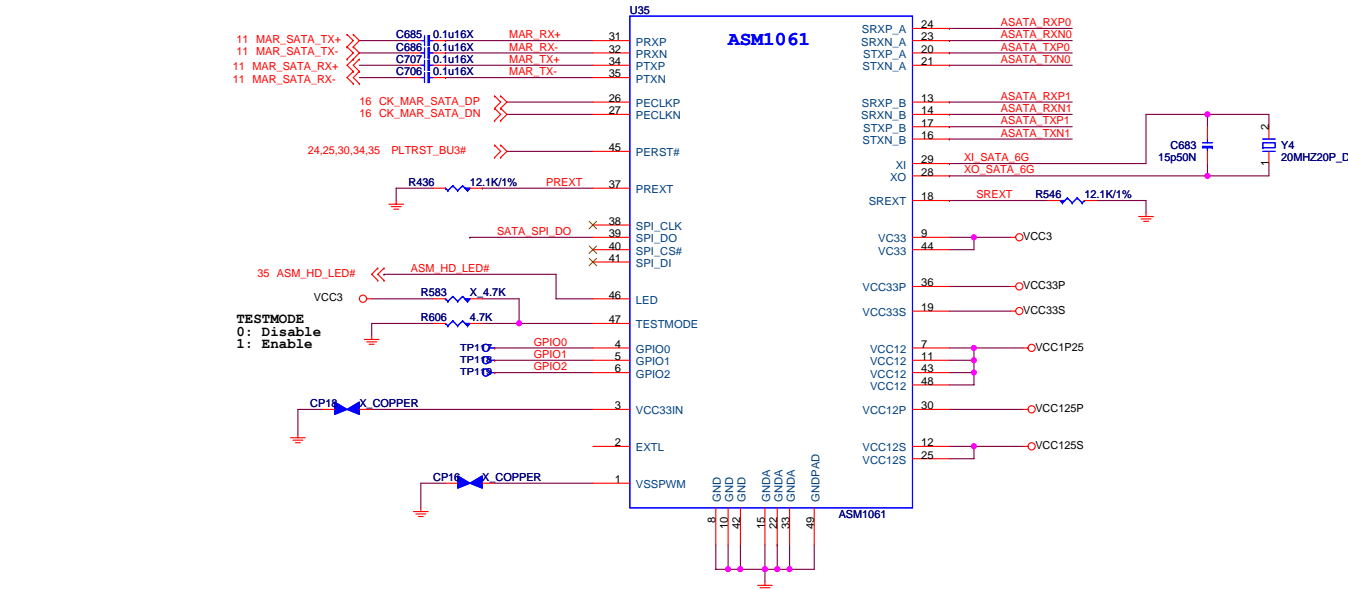


close to Connector close to Connector

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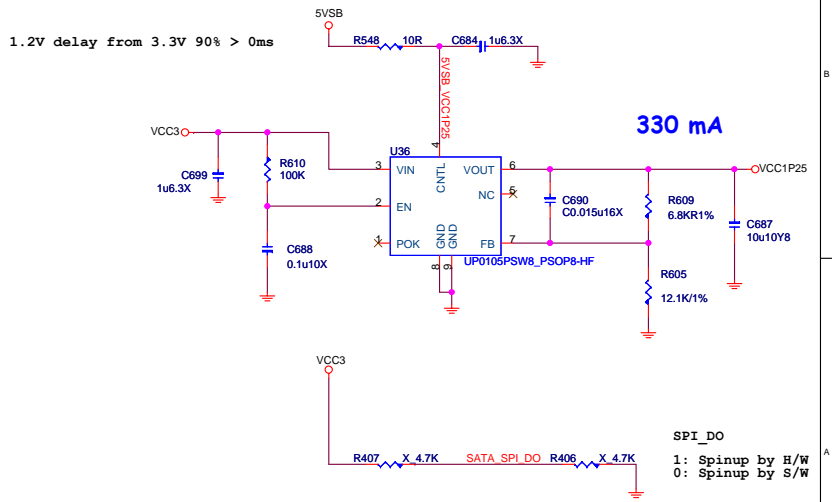
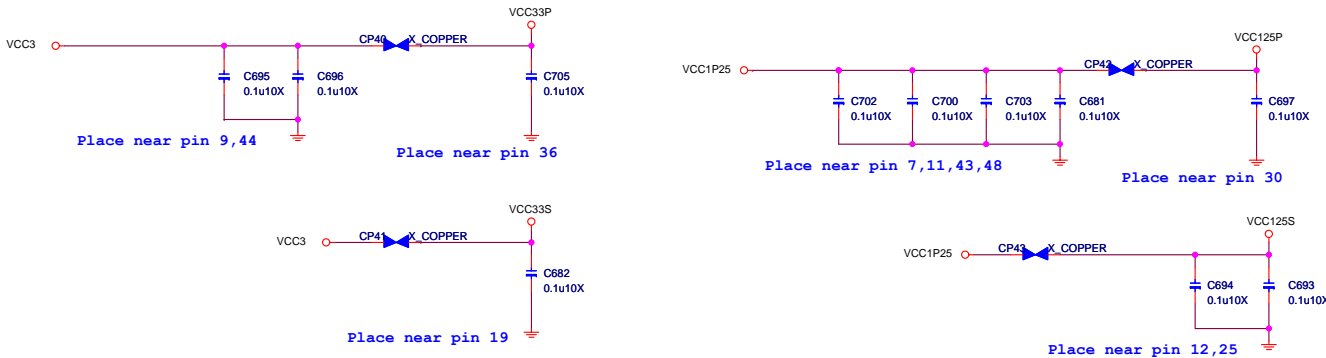



ASM1061 SATA6G



ASM1061 POWER Consumption

	3.3V	1.2V	Power (mW)
Idle (mA)	98.45	212.3	579.645
Busy (mA)	91.1	330.7	697.47



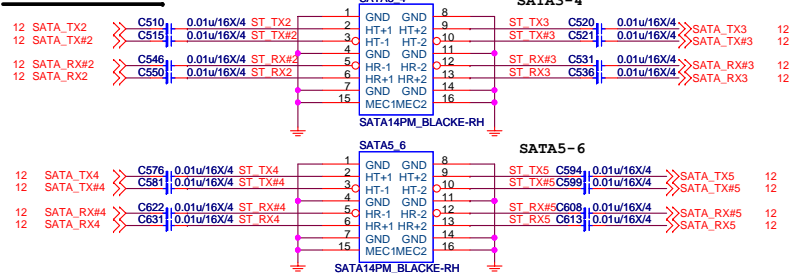


MICRO-STAR INT'L CO.,LTD

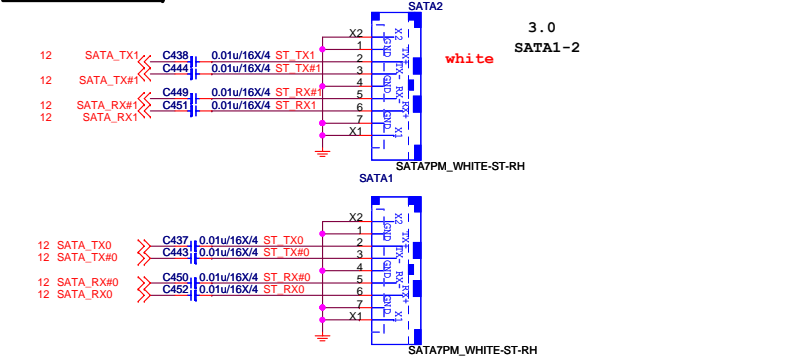
MS-7736

Size	Document Description	Rev
Custom	ASM1061 SATA6G	10
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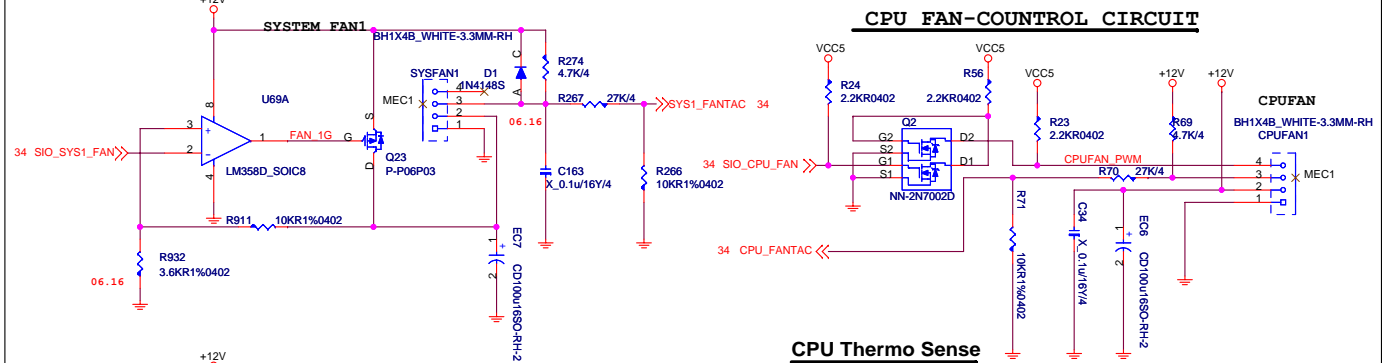
SATA2 Ports



SATA3 Ports



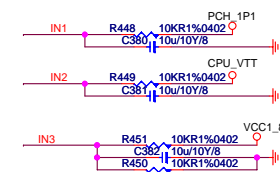
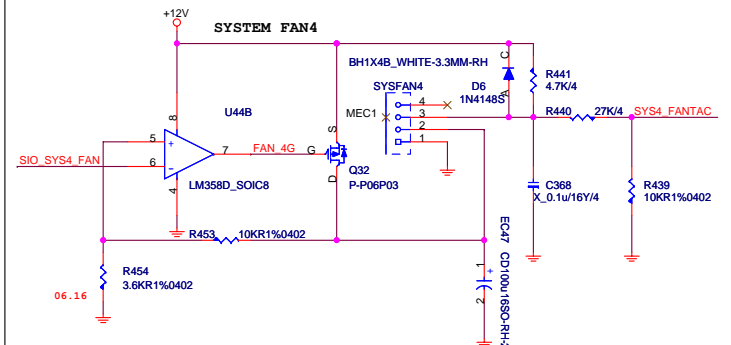
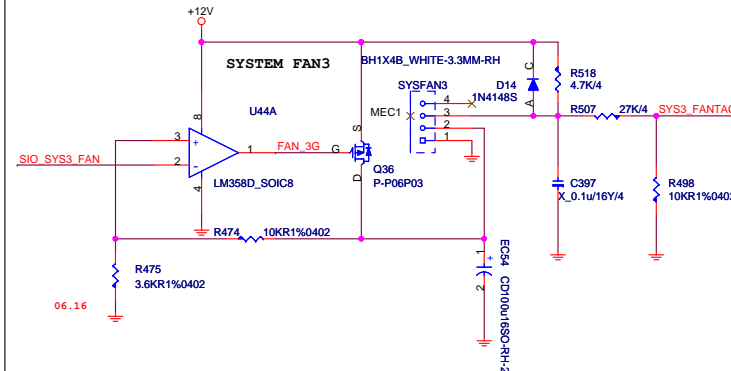
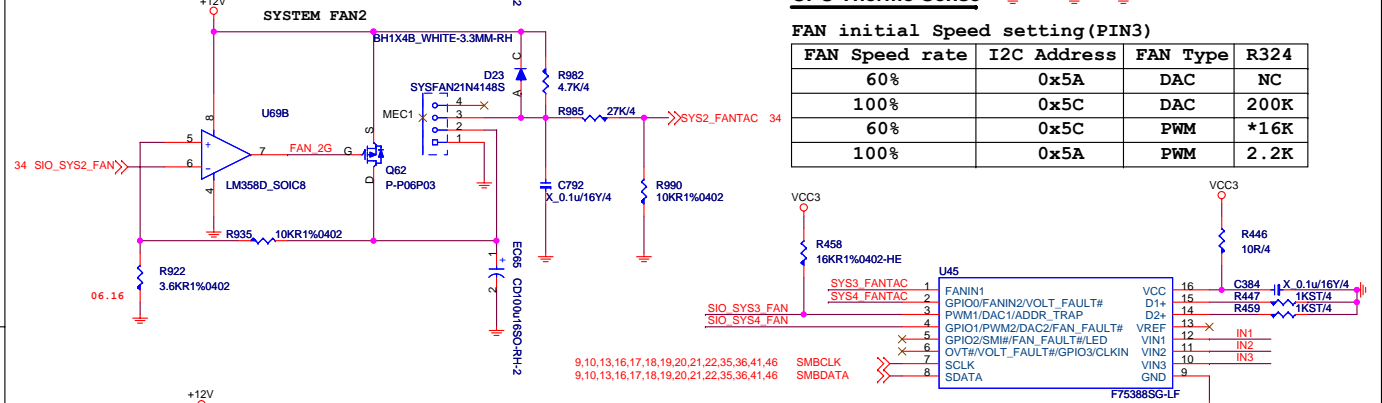
CPU FAN-COUNTROL CIRCUIT



CPU Thermo Sense

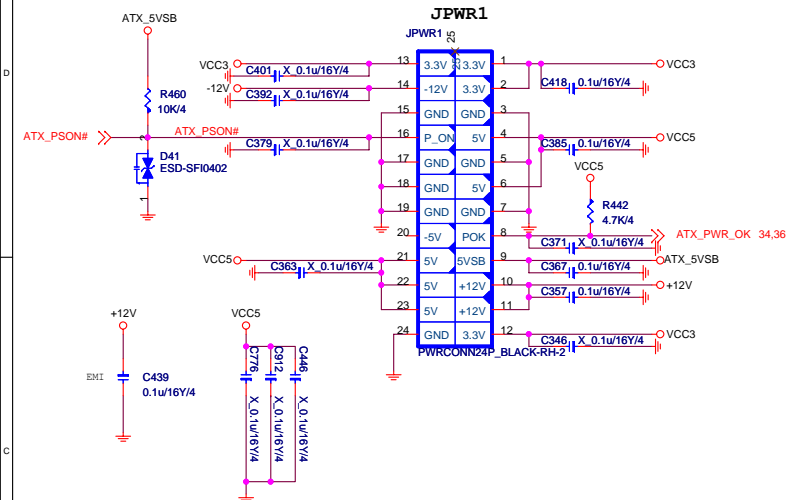
FAN initial Speed setting (PIN3)

FAN Speed rate	I2C Address	FAN Type	R324
60%	0x5A	DAC	NC
100%	0x5C	DAC	200K
60%	0x5C	PWM	*16K
100%	0x5A	PWM	2.2K

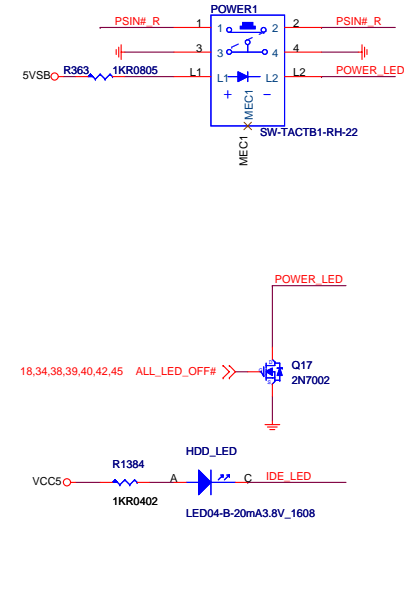
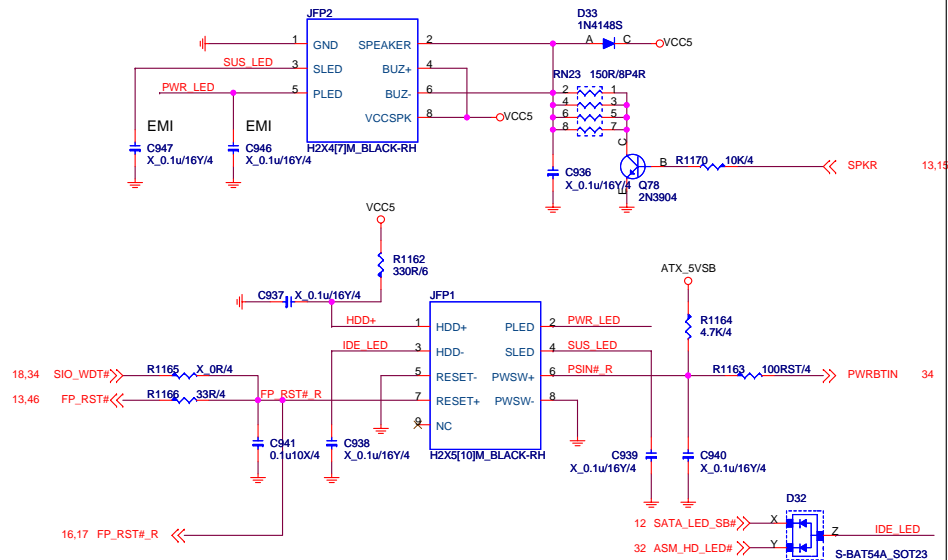


HW Monitor

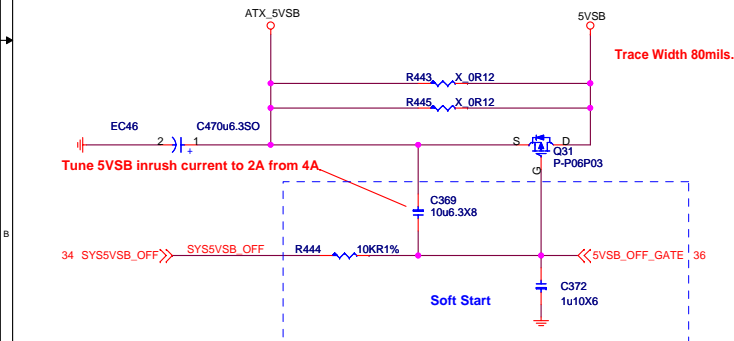
ATX POWER CONNECTOR



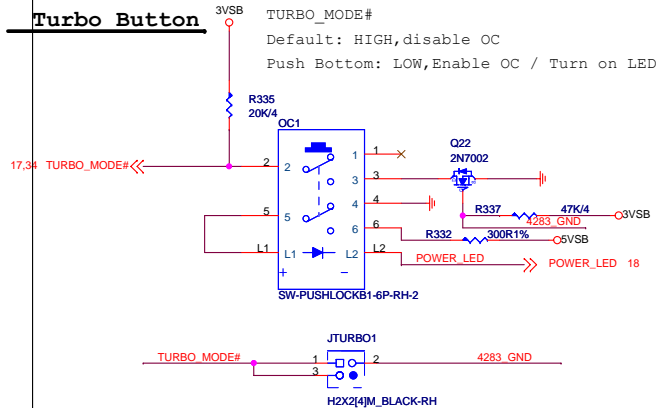
FRONT PANNEL



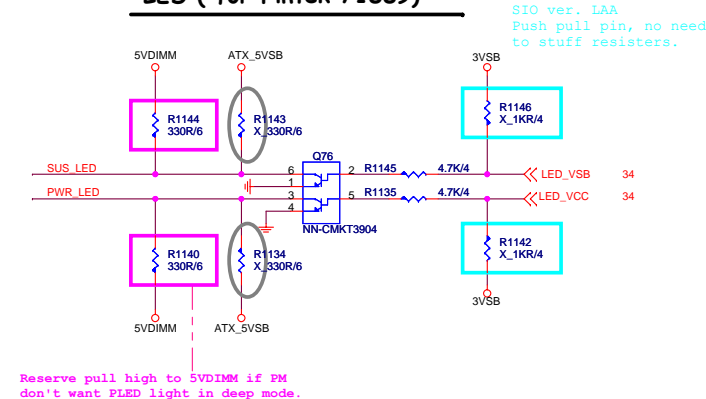
5VSB Power Switch



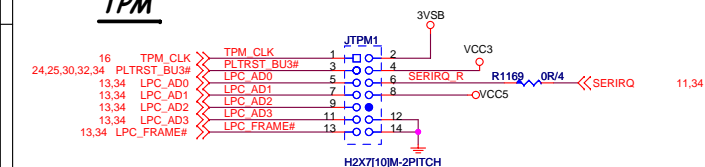
Turbo Button



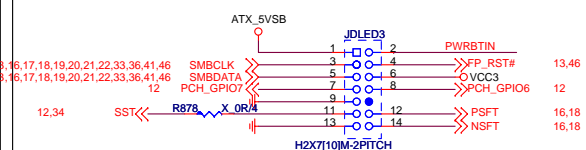
LED (for Fintek 71889)



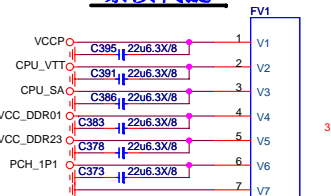
TPM



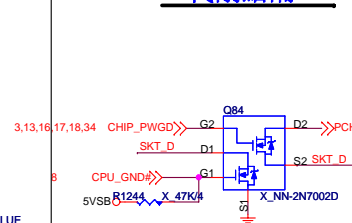
JDLED3



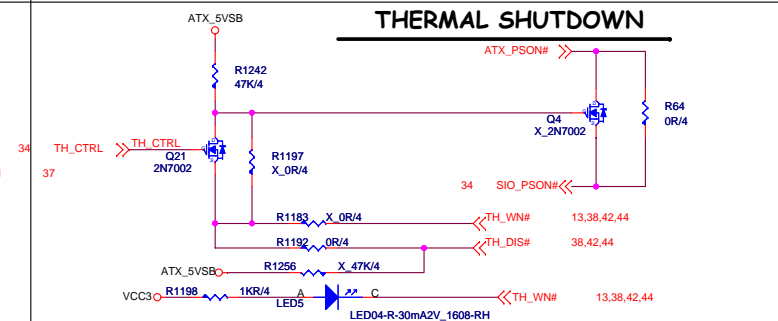
策潰代鏈



ǎ代剛結隔



THERMAL SHUTDOWN



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5VDIMM FOR DDR

VCC5 ○ R298 510R/4

34,35 ATX_PWR_OK >> R292 10KR1%0402 5VDIMM 5V

13,18,34 SLP_S#* >>

18,24,25,34,39 SLP_S#* >> R299 OR/4

34,39 SLP_SS_LCH# >> R306 X OR/4

If you use LAA and can support dcmpp s3,
please use SLP_S5_LCH#,else use SLP_S#*.

U21
S3#
S5#
5VCC
5VSB
5VSB_DRV
MODE
GND
5VCC_DRV
uP7501

R313 10R/4 ATX_5VSB

C195 0.1u/16X/4

G3

5VSBDRV1

D

S1

VCC#

C27 NP-P2003ND5G TO252-5 5VDIMM

C218 0.1u/25V/4

+12V

R315 1K/B/1

C201 22n/16X/4

C190 18n/16X/4

ATX_5VSB

Read SLP_S5# for AMT

7501 Mode
H:Support S0/S3/S5
L:Support S0/S3

If you use LAA and can support deep s3,
please use SLP_S5_LCH#,else use SLP_S4#

Used SLP_S5# for AMT

7501 Mode
H:Support S0/S3/S5
L:Support S0/S3

UPI_VOLTAGE_CONSOLE

0x24 : RH=11K, RL=15K

ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (Kohm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

5VSB_1811

R1194 0R/4 5VSB_1811

C466 0.1u/16Y/4

R949 15K/1%0402

R966 11K/1%0402

UPI1811BMA8

PCHIP1_FB 37

PCHIP5_FB

SMBCLK

SMBDATA

VCC

BUS_SEL

SCL

SDA

GND

OUT1

OUT2

OUT3

0,10,13,16,17,18,19,20,21,22,33,35,41,46

1,2,3,13,16,17,18,19,20,21,22,33,35,41,46

0x24: RH=11K, RL=15K						
ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (Kohm)	OPEN	3.9	3	2.2	1.3	10
RL (Kohm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

[illegible][illegible]

PCH1.5

512mA

uP7536 SLP_S3#

26,27,28 5VDRV1_EN

5VDRV1 R1137 200K/1% 50402

R552 68K/1%

VCC3

R656 1K/1%

R709 X_4.7K

ATX_5VSB

R713 47K

Q49 2N7002

Q52 2N7002

C251 0.1u16X

5VDIMM 5V

Patch coolermaster 700w power sequence

Patch coolermaster 700w power sequence

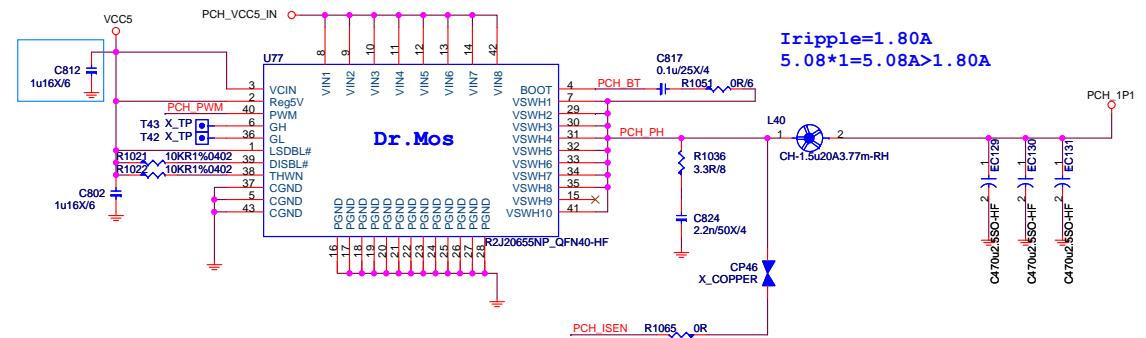
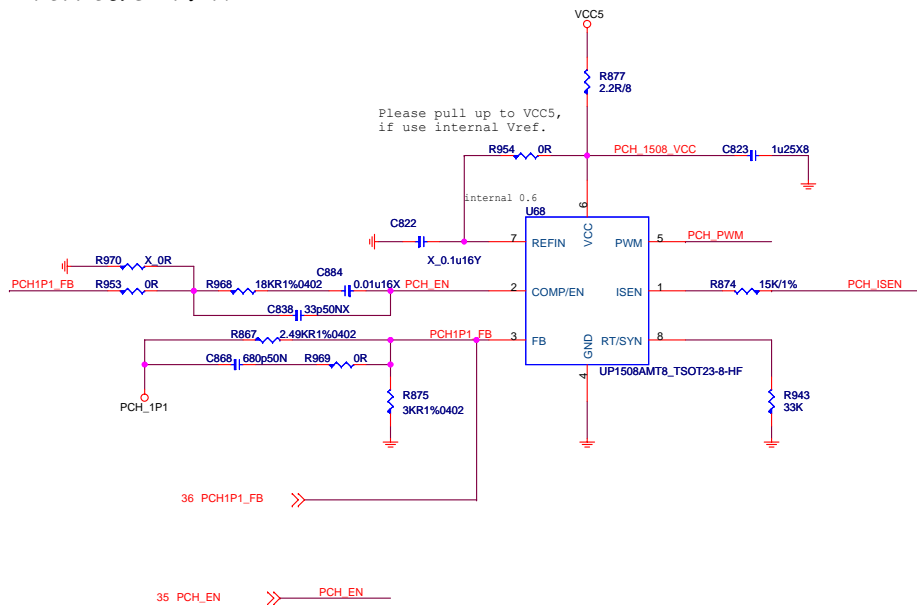


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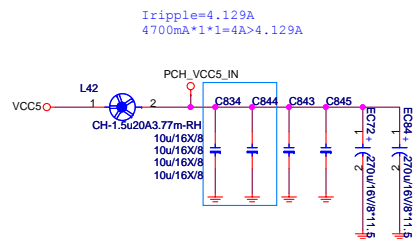
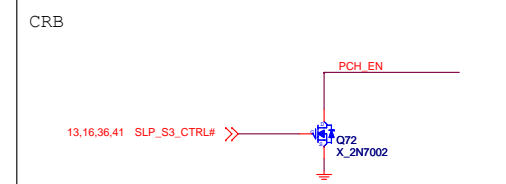
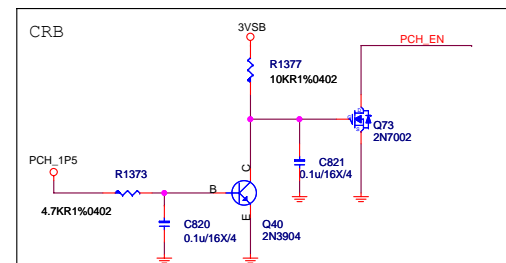
Size Custom	Document Description ACPI controller UPI	Rev 10
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PCH Core 17.2A

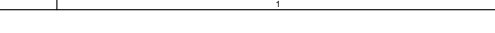
Please pull up to VCC5,
if use internal Vref.



Iripple=1.80A
5.08*1=5.08A>1.80A



DDR3_1.5V 20A



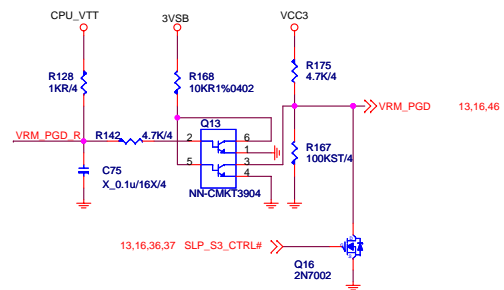
Size Custom	Document Description DDR01-uP6212 2-Phase	Rev 10
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1

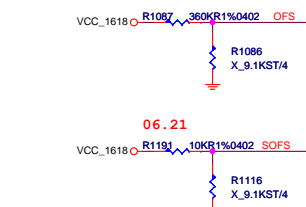
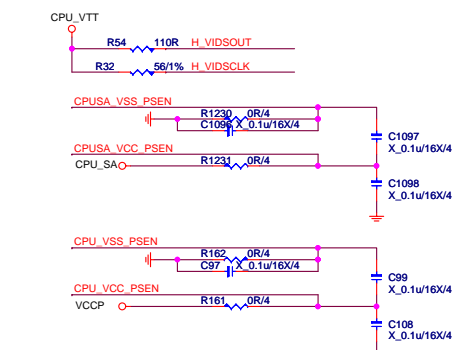
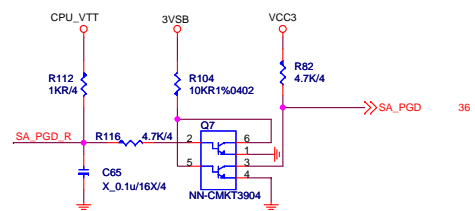




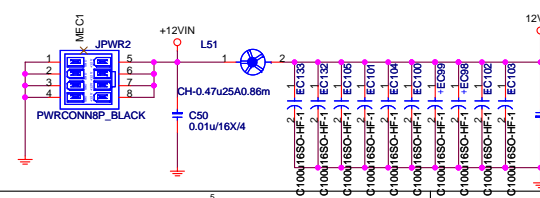
VRMPWRGD LEVEL SHIFT



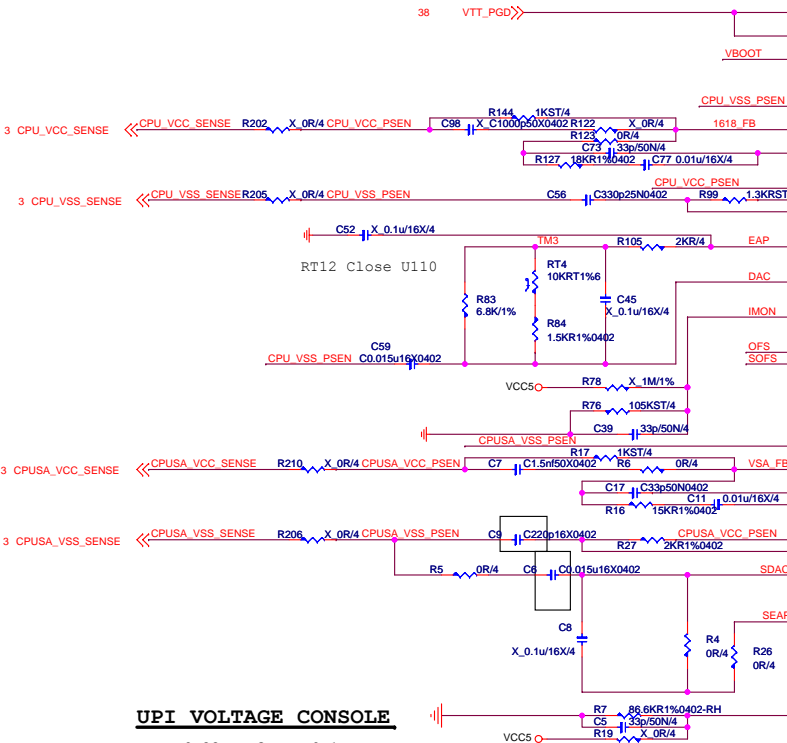
SAPGD LEVEL SHIFT



$$5000\text{mA} \times 4 \times 1 = 20\text{A} > 13.7\text{A} \quad (7.68)$$



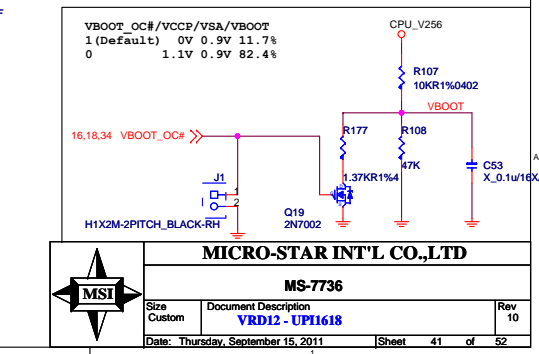
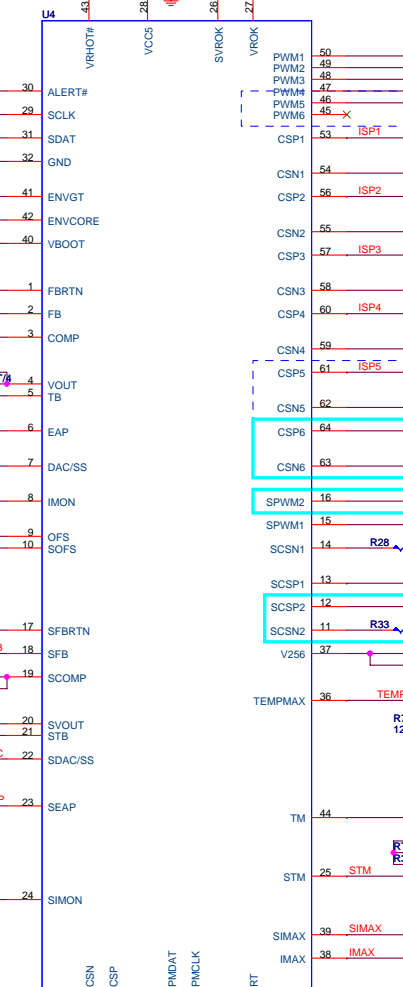
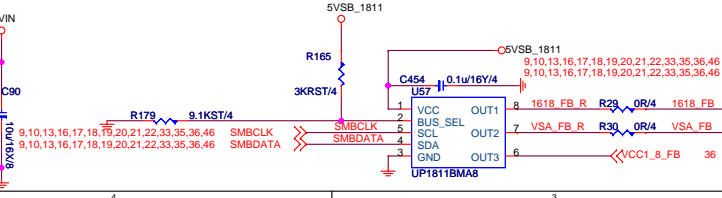
3000mil < L < 6000mil
4mil / 20mil
55 ohm Impedence
must be Referenced GND



UPI VOLTAGE CONSOLE

0x22: RH=3K, RL=9.1K

ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (Kohm)	OPEN	3.9	3	2.2	1.3	10
RL (Kohm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

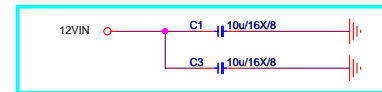
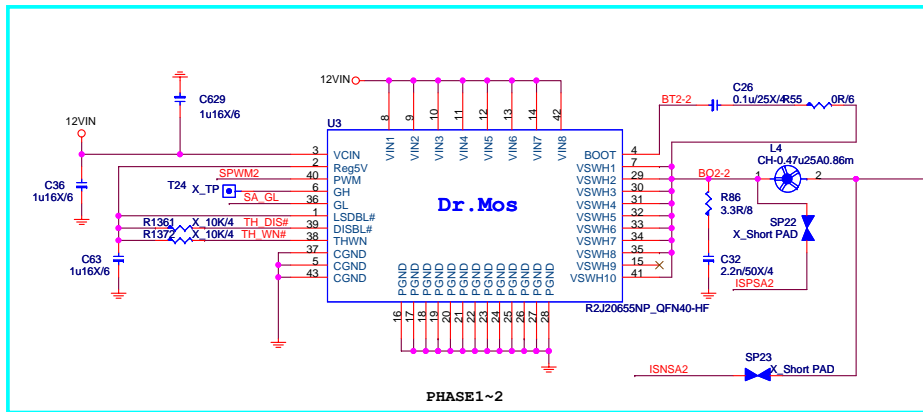
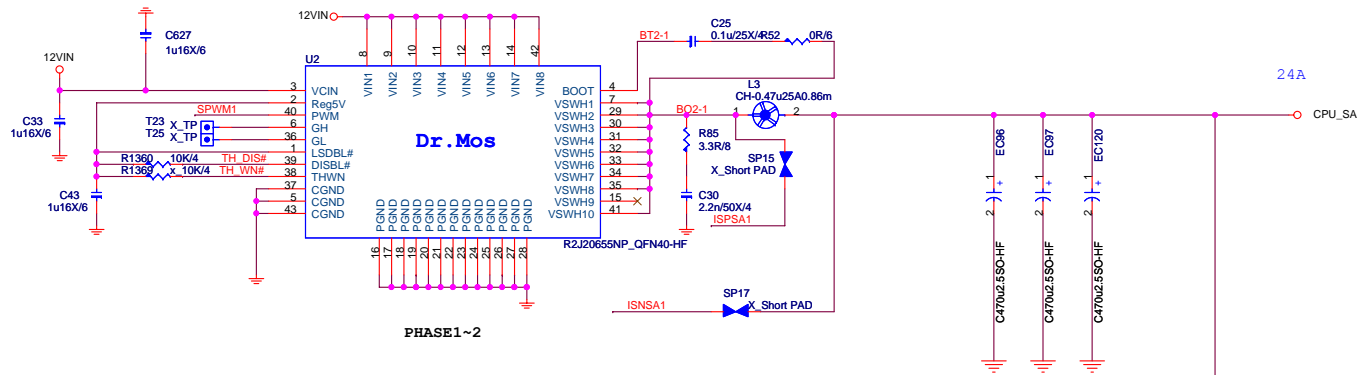


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		VRD12 - UPI1618	10

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41 ISPSA1 >>>
41 ISNSA1 >>>

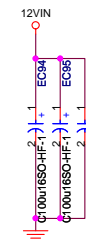
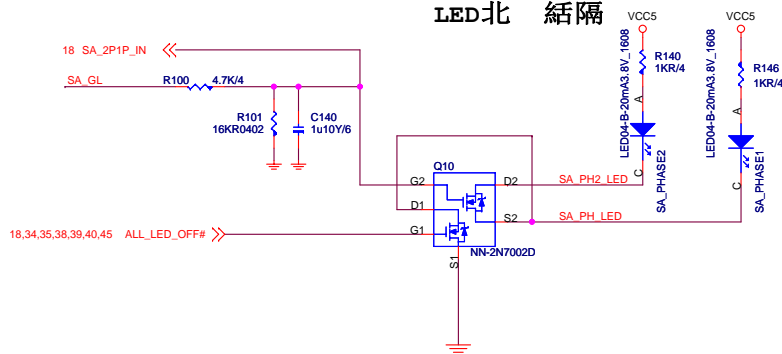


41 SPWM1 >>>
41 SPWM2 >>>

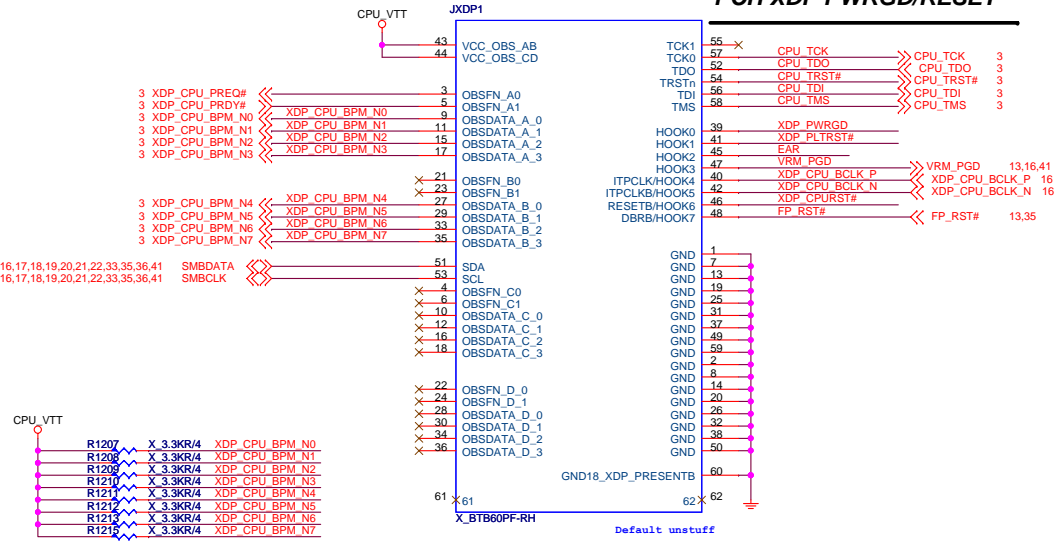
LED北 結隔

13,35,38,44 TH_WN# <<< TH_WN#
35,38,44 TH_DIS# <<< TH_DIS#

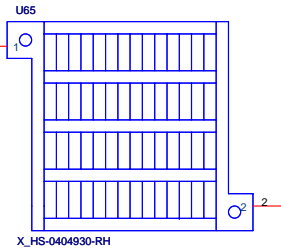
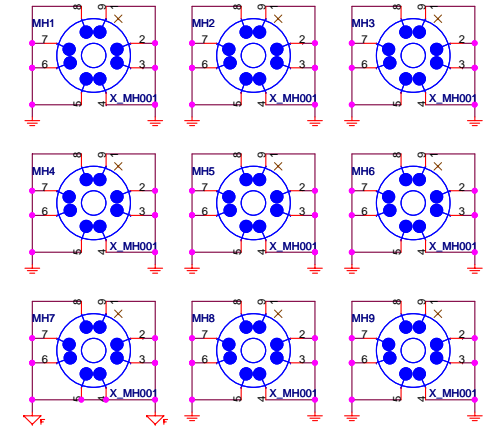
LED北 結隔



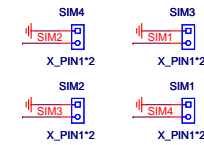
PCH XDP PWRGD/RESET



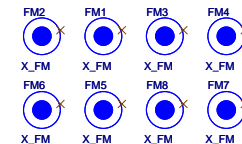
Mounting Holes



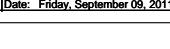
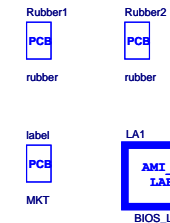
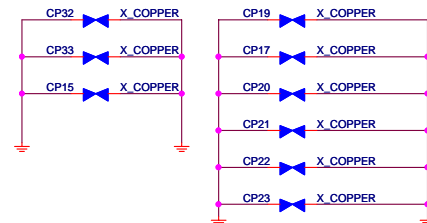
Simulation



Optical Fiducial Marks-120



Optical Fiducial Marks-100



PK0-077350B-G37, 紋 不

JP3 PCH HEATSINK

JP4 MOS HEATSINK

JP1 Down Steel

JP2 Upper Steel

X_CPU_H1 CPU

X_CPU_H1

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